3D InCites YEARBOOK

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Interconnectology Saves the World!

By Françoise von Trapp

In 2007, when I was managing editor at the now defunct *Advanced Packaging Magazine*, we went out on a limb in our January Industry Forecast to declare, as our cover story: *Advanced Packaging Saves the World!* In 2008, we tempered that declaration to *Advanced Packaging Drives the Industry*! By 2009, we were in the midst of a downturn, and the January cover story was titled *Weathering the Storm*. Halfway into January, the magazine folded.

Despite that, I never lost faith in the promise of advanced packaging. I staked my career on it by launching 3D InCites in July 2009. Were we clairvoyant? I'd like to think we were just paying attention. Fan-out wafer-level packaging and 3D integration technologies were in the early stages of development, and we followed them closely. While most of the semiconductor industry was still in hot pursuit of Moore's Law, EUV lithography, and 450mm wafers, we were focused on through-silicon via (TSV) fabrication and emerging developments in hybrid bonding.

Nonetheless, it was never really the packaging part that would save the world. It was the emerging advances in interconnect technology that caught the attention of the semiconductor industry as traditional CMOS scaling slowed. How do we improve power, performance, area, and cost? Chiplets are the answer and advanced interconnect processes that make them possible. Imec's Luc Van den hove calls it CMOS 2.0. We call it Interconnectology.

Now, as regions around the world race to be leaders in semiconductor manufacturing, they also recognize that advanced packaging and interconnectology are the keys to it all. The semiconductor industry and governments worldwide recognize this. Investments in advanced packaging innovation were the big stories in 2024 and will continue to be so in 2025. That's why we dedicated a special cover section to *Advanced Packaging Around the Globe* in this issue of the 3D InCites Yearbook.

Our newest technology blogger, Jillian McNichol, kicks things off with her article, *"How Arizona is Growing its Advanced Packaging Capabilities"*. She paid visits to several of our members located in the Greater Phoenix area to learn how the state's investments are impacting them. In *US-JOINT Consortium: Strengthening Semiconductor Innovation Across Borders* 3D inCites intern, Avery Gerber interviews our community members participating in this collaboration organized by Resonac. Dean Freeman provides his market researcher perspective with *Advanced Packaging in Asia*. Spoiler Alert: the region still reigns supreme for advanced packaging. I report back from visits to two member companies that are expanding operations in the Midwest and East Coast: NHanced Semiconductors in Odon, Indiana, and Raleigh, North Carolina; and Onto Innovation with its PACE Center in Massachusetts.

This special section also features contributed articles by members of the 3D InCites community. IBM's Dr. Scott Sikorski provides an update on advanced packaging in the Northeast Corridor. EV Group's Paul Lindner helps us navigate the European chip renaissance. Frank Windrich and Juliana Panchenko celebrate Fraunhofer IZM-ASSID's 15th anniversary with the article, *Fraunhofer: The White House of Advanced Packaging*.

The issue also features contributions on other topics that were top-of-mind for 2024. You'll get an update on the PFAS situation from Julia Freer. Jim Straus, of ACM Research writes about what's driving the move to panel-level packaging. Tony Mastroianni and Todd Burkholder, Siemens EDA bring you the latest update on taking 3D IC heterogeneous integration mainstream.

Isabella Drolz, Comet Yxlon writes about closing the gap on the European talent shortage. Henkels' Ram Trichur describes the benefits of attending industry events, and Texas A&M senior, Camden McCrea, shares his experience as an intern with IMAPS and attending the IMAPS Symposium.

Simon McElrea, who, along with Scott Jeweler, helped coin the words interconnectology and interconnectologist, once told me that to him, interconnectology means more than a toolbox of interconnect solutions – it means inter-company collaboration.

We couldn't agree more. That's why 3D InCites is more than just a platform. It's a community of interconnectologists. So we've launched some networking events adjacent to major conferences to foster that community feel. In March, in addition to our annual 3D InCites Awards ceremony, we held the first BackYard Olympics in collaboration with the IMAPS Device Packaging Conference. In November, the day before SEMICON Europa, we celebrated all things interconnectology at the 3D InCites Member Stammtisch and the inaugural Interconnectology Eisstockschiessen Invitational hosted by LQDX. Check out the *Year in Pictures* to see how much fun we had making connections at all these events. We're already looking forward to continuing these traditions in 2025.

So in more ways than one, this issue celebrates all things interconnectology. Will it save the world? Who knows. But one thing is for sure, we're going to have fun trying.

Cost-effective, High-performance Chips Are Driving the Move to Panel-level Processing

By Jim Straus, ACM Research

Artificial intelligence (AI) is driving the need for faster processing speeds to keep up with the large language models. As a result, we see multi-reticle packages using 2 x 800 mm^2 chips in production in a single package. These larger chip sizes and the need for better yields and higher capacity drive the move from wafers to larger rectangular substrates for the packaging process. The move to fan out panel-level packaging (FOPLP) is partly driven by the industry's move to packaging chips on a substrate to reduce the limitations and constraints of the wafer-level packaging process. The rapid adoption of multiple-reticle chiplets has created packaging shortages as the FOWLP packaging process is capacity-constrained due to the large size of these packages.

To improve the capacity situation, packaging companies are working to develop panel-level packaging (PLP). Instead of using a round wafer in the packaging process, a square substrate will be used for PLP. AMC Research (AMCR) has a long history of success with wafer-level packaging (WLP), and it is supporting the transition to PLP with new approaches for cleaning and deposition technologies. Before we move into some details of PLP, however, let's discuss why we need to move to larger substrates in the first place.

Large-package Design Challenges

Building packages that are larger than 2 x 800mm^2 has multiple challenges. One of the biggest issues is how many 800mm^2 chips can be placed on a 300 mm wafer or packaging substrate. With a chip size of ~800mm^2, about 64 chips can fit on a round 300mm wafer. However, this does not consider yield. The chip is square and the wafer is round, so a significant amount of substrate goes to waste in the chip's processing. This is because a considerable amount of area at the edge is lost due to the mismatch in shape.

To help resolve packaging supply chain constraints, the packaging industry is moving from round substrates to square panels. Both wafer manufacturers and outsourced assembly and test (OSAT) packaging suppliers have proposed using square glass panels as the substrate for packaging the large-area chiplets. This will significantly increase the number of chips that can be processed on a single panel and should ease current supply constraints. The industry for now has settled on panel sizes of 515mm x 510mm, which has 3x the area of a 300mm silicon wafer; and 600mm x 600mm, which has 5x the area of a 300mm wafer (Figure 1).

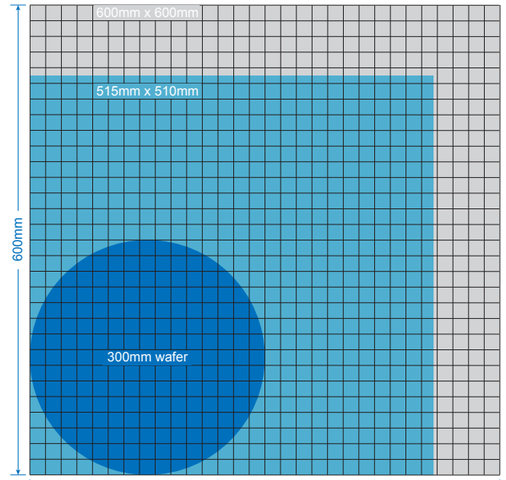


Figure 1: 300mm wafer compared to 515mm x 510mm and 600mm^2 panels

Advantages of Panel-level Packaging

Transitioning to PLP has some advantages over WLP. For example, PLP enables the industry to significantly increase the substrate area for building chiplets, improving yield and lowering packaging costs. The larger area allows more chips to be assembled simultaneously, increasing capacity and thus reducing the current supply constraints. FOPLP will allow for the integration of various die technologies (e.g., logic, memory, and RF) more easily in a single package, which supports more complex system designs.

Continued on page 69

What You Need to Know About PFAS

By Julia Freer, JLFG Communications

You have probably heard about health and environmental concerns related to per- or polyfluoroalkyl substances (PFAS). Companies are being pressured to replace PFAS with safer alternatives for nonstick coatings, water-resistant fabrics, firefighting foams, and more to meet upcoming restrictions. For manufacturers, including those in the semiconductor industry, PFAS replacement is incredibly complicated.

The Proliferation of PFAS

PFAS are used in nearly every step of the semiconductor manufacturing process, from lithography through packaging. This isn't merely a concern for companies making and purchasing process chemicals. The consequences of PFAS use apply to every company in the industry, whether a facility makes chemicals, materials, equipment, or components. Even companies that outsource all their manufacturing probably have PFAS in their buildings, and they should also know what their vendors are doing.

Some applications of PFAS are common to multiple manufacturing sectors. Items such as tubing, fittings, cables, filters, valves, pumps, lubricants, and power supplies are relatively universal. The semiconductor industry can learn from what other sectors are doing to replace PFAS and join forces to advocate for PFAS-free supplies and components. However, what works for, say, industrial or automotive sectors might not be high enough purity to be compatible with semiconductor particle contamination limits.

Other PFAS uses are industry-specific. Fluorocarbon gases are required to etch silicon. Photoacid generators (PAGs) and etchants containing PFAS enable 193mm and UV lithography. The list goes on. Research into PFAS-free alternatives is ongoing, but we are still many years away from workable substitutions that meet yield, performance, and productivity requirements.

Companies should continue R&D efforts to replace PFAS and invest enough to accelerate progress. Meanwhile, there are several urgent issues that our industry needs to consider related to newly enacted and upcoming legislation about PFAS.

The Regulatory Environment

As legislation restricting the use of PFAS proliferates, action is becoming a matter of compliance. While most of the proposed laws banning PFAS target consumer goods, there are several issues for our industry to consider: reporting requirements, wastewater treatment, and supply chain risk. But first, let's talk a bit about existing and pending legislation.

The widespread PFAS ban that the European Chemical Agency (ECHA) proposed in early 2023 is still under discussion. SEMI and the European Semiconductor Industry Association (ESIA) were among many industry groups that submitted feedback. They requested a 12-year derogation for the entire semiconductor industry supply chain. This is based on the critical role that our industry plays in multiple end markets and the difficulty in replacing PFAS in our manufacturing processes.

The regulatory situation in the U.S. is complicated by a multitude of laws that are in effect or under consideration in over half the states. A search of legislation with the keyword "PFAS" results in over 500 entries for federal and state measures. I attempted to review legislation intending to restrict PFAS use and quickly became overwhelmed.

The map in Figure 1 color-codes states according to the most extensive bill passed or under review. Some states that intend to restrict PFAS in many categories of consumer products, for example, also have laws relating to wastewater management, firefighting foam, or PFAS monitoring. (Caveat: I don't guarantee that the map is 100% correct, but it gives an idea of the scope of PFAS legislation.)

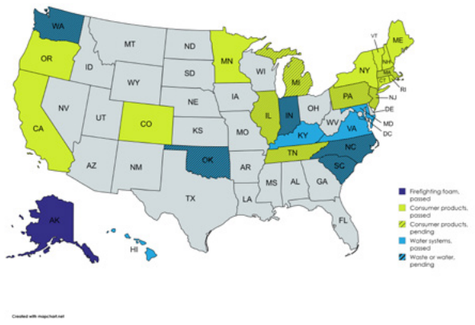


Figure 1: U.S. Map Highlighting states with passed or pending legislation regulating PFAS use

A recently passed law in Minnesota is the most far-reaching to date. It bans PFAS in eleven categories of consumer products beginning January 1, 2025, and in "any product that contains intentionally added PFAS" in 2032, with an exception for "currently unavoidable use." Laws in several states, including California, Oregon, and New York, restrict PFAS in one or more consumer product categories as of January 2025. Other similar state restrictions will take effect in 2026. Pending laws in several states mimic the wording of the Minnesota bill.

Most state-level bills aim to eventually phase out all "unavoidable" PFAS use, though they don't clarify how they determine whether a use is unavoidable. The bills start with bans on intentionally added PFAS in specific consumer goods categories, as noted above, with provisions five to eight years out that extend to unintentionally added PFAS and to any product where substitution looks possible. The broadest restrictions will take effect between 2030 and 2032. Figure 2 presents a general timeline.

As of October 2024, Maine's bill is the only one to specifically list semiconductors as a product category exempted from the 2032 PFAS phase-out. Other states will likely follow suit before the broadest restrictions come due.

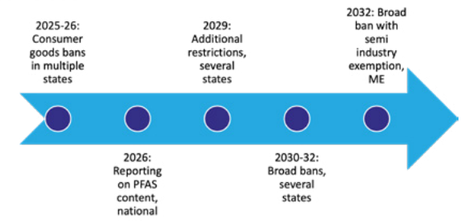


Figure 2: Timeline of passed and pending PFAS regulations

Reporting

For companies outside the consumer goods industry, the immediate need is to plan for reporting requirements from the U.S. Environmental Protection Agency (EPA) that will take effect in January 2026. Some states have separate reporting laws, but federal law may override those. According to the EPA requirements, companies will need to report on their PFAS usage dating back to 2011. Any entity that manufactures PFAS chemicals or PFAS-containing products is obligated to collect and share a multitude of data, including:

- The quantities of each specific PFAS used and how it is used in the manufacturing process
- Description of byproducts resulting from manufacturing, processing, or disposal
- Environmental and health effects of all PFAS-containing substances or mixtures
- Plans for disposal of all of the above

If you don't have a plan for generating and tracking the data, it's time to start. Data collection will require tracking suppliers of all chemicals and components to discover whether those items contain PFAS. The EPA's 138-page reporting instructions document contains all the details.

Wastewater

From a public health perspective, keeping PFAS and other toxic chemicals out of our soil, water, and air is critical. PFAS laws relating to water systems or waste treatment are also relevant to our industry because they apply to any facilities in the state regardless of what they make or what industries they serve. Discharge of PFAS-containing waste, whether accidental or not, can carry fines or get a company sued.

A New Hampshire bill, which the governor signed in August 2024, exposes any PFAS facility releasing hazardous waste containing PFAS into ground or surface water to liability. The concentration that triggers the regulation is 10 parts per billion (ppb). The bill, which also restricts PFAS in consumer goods, defines a PFAS facility as "any site, area, or location where PFAS is or has been used in a manufacturing process."

The best way for a fab or other manufacturing facility to ensure they don't run afoul of water-related PFAS regulations is not to release these chemicals into the environment. A combination of on-site filtering and recycling can accomplish this goal. Something as simple as installing activated charcoal water filters or reverse osmosis systems can stop PFAS from entering the public water system. Water testing will verify if your filtration is sufficient.

Supply Chain Risk

Even legislation that does not directly restrict the use of PFAS in semiconductor manufacturing can affect our industry if we cannot procure these chemicals. In late 2022, 3M announced its intention to exit PFAS manufacturing by 2025, and the company intends to follow through. Given 3M's history of supplying PFOA and its $10-12 billion settlement to support remediation of PFAS in US public water supplies, the move makes sense for the company even without the demands of the Minnesota law prohibiting PFAS manufacturing.

The question is how 3M's move will affect the supply chain. Its customers will be forced to switch suppliers, perhaps outsourcing to countries without strict environmental regulations regarding disposal and wastewater treatment.

Regulations restricting PFAS use in consumer goods may also affect the cost and availability of these chemicals in our industry. Suppliers threatened with lawsuits may decide to exit the market or indirectly pass the cost of legal bills to their customers. As a minor player in the global PFAS market, semiconductor companies have limited clout. For example, the semiconductor industry buys a tiny percentage of global production of several fluoropolymers that are used extensively to make all sorts of equipment. It may be especially hard to secure shipments of these materials.

Do Something

It's a good idea to understand your company's risk regarding PFAS. Do you know what PFAS are in your facilities? Have you contacted suppliers to learn about potential supply chain disruptions due to pending PFAS regulations? Do you know what's in your wastewater?

If you want to stay abreast of the ever-changing regulatory landscape and have a say in our industry's response to PFAS risk, you can participate in one of SEMI's PFAS working groups or the Semiconductor Industry Association's PFAS Consortium. Dozens of companies in our industry are involved in discussions around supply chain resiliency, transparent communication, and transition strategy. The long-term goal is to finalize an industry roadmap for PFAS detection, replacement, and remediation, along with standardized communication to ease the burden of meeting reporting requirements.

Taking 3D IC Heterogeneous Integration Mainstream

By Tony Mastroianni and Todd Burkholder, Siemens EDA

Over the last several years, chiplet-based heterogeneous package integration has emerged as a promising alternative to traditional monolithic package solutions; the so-called homogenous SoC design. 3D IC heterogeneous integration is a system approach, wherein what typically would be implemented as an SoC is disaggregated into solid, fabricated IP blocks; i.e., *chiplets*.

These chiplets typically provide a specific function implemented in an optimal chip process node. Several chiplets and an optional, custom SoC device can be mounted and interconnected in a single package using high-speed/bandwidth chiplet-to-chiplet interfaces. The resulting 3D IC heterogeneously integrated packages deliver greater performance at a reduced cost, higher yield, and have only a slightly larger area than a traditional monolithic SoC package.

This system-oriented approach, known as system technology co-optimization (STCO), differs from traditional IC design. STCO spans five significant activities that are both complex and sophisticated: architectural planning and analysis, functional design and test, physical design planning and verification, and electrical and reliability analysis.

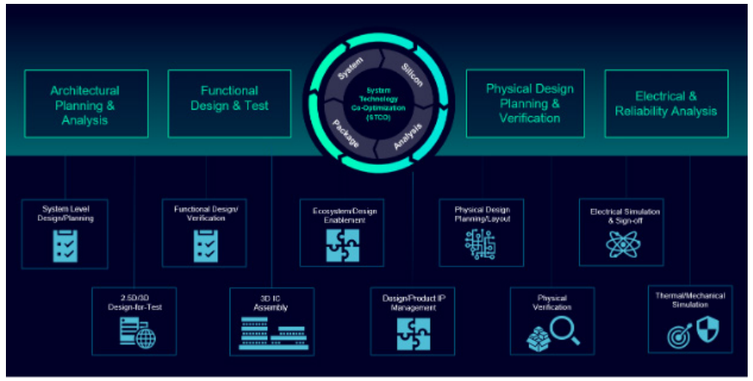


Figure 1: 3D IC heterogeneous integration requires a co-design and co-optimization approach (STCO).

With this new approach come many advantages, opening new possibilities in electronic system design; however, the question facing us is how to facilitate the adoption of this exciting yet esoteric 3D IC methodology, one requiring a high degree of expertise and effort.

With that quest in mind, in 2021, the Chiplet Design Exchange (CDX) was established within the Open Compute Project (OCP) to promote and support this technology and eventually deliver it to the mainstream. The CDX group comprises EDA vendors, Fabs, OSATs, and substrate material providers. The charter of the CDX group is to promote a chiplet ecosystem by defining models that are necessary to support the 3D IC design process, as well as the different types of design kits that this requires. Therefore, we set out to establish an ecosystem of design kits to enable 3D IC design throughout the semiconductor industry and address the fact that the packaging community has lacked the well-structured design kits and PDKs available for traditional ASIC technologies.

The idea was that we could eventually have reusable chiplets out in the marketplace, and that's what we're promoting in the CDX group. Therefore, it was critical to develop and leverage existing standards for the various 3D IC design kit formats (which we call 3DKs), and we wanted the 3DKs to be in machine-readable formats that can be consumed by the tools and the workflows. In turn, we needed to have the EDA companies support these workflows and the different formats. Finally, to make the critical link to manufacturing, the OSATs—the foundries that generate the data for these different design kits—also had to be part of this ecosystem.

The 3DKs: 3D IC Design Enablement

As mentioned, the IC design process has a very structured, well-defined design enablement infrastructure. It includes IP: the reusable building blocks of SoC designs. There are process design kits, which include the technology rules for creating extraction decks, place and route decks, et cetera. There are also macros for memory and analog signal-type designs. We're trying to extend that concept for many things in the packaging world, but a different set of design kits is required. So, 3D IC design requires a comprehensive set of new design enablement kits to support the design, verification, and handoff to manufacturing.

These design enablement kits fall into five key areas, as reflected above. These are physical design, electrical

analysis, reliability analysis, and test that start up front during planning. Also, as parts are delivered for manufacturing, test factors both for the individual chiplets as well as the complete system-in-package (SiP) must be generated.

To support the needs in all these key areas, we are developing four 3DKs to provide a comprehensive set of design enablement kits that support the design, verification, analysis and testing of 3D IC designs.

- **Chiplet Design Kits (CDK):** Recommended chiplet models to support the integration into a 3D IC design
- **Package Assembly Design Kits (PADK):** Chiplet IO/TSV pitch spacing rules, substate/interposer width/spacing, routing rules, and general-purpose package component placement rules
- **Material Design Kits (MDK):** Composite material properties for package components to support electrical and reliability analysis
- **Package Test Design Kits (PTDK):** Defines test IO pins, dimensions, and function to support ATE test hardware and testing

Chiplet Design Kits

CDK models are created or reused for early architectural, test, and physical design planning. These are the models that are required to design a chiplet. So, the first thing the CDX group did was determine the design models required to integrate a chiplet into a package. Our first effort involved working with the JEDEC group.

The JEP30 PartModel was designed to describe electronic components used in a PCB design. As we were trying to do a similar thing for 3D ICs, we asked them to help us extend that part model to support chiplets. Together we came up with a list of chiplet design models that we recommend be included with a chiplet. The idea is that we could eventually have reusable chiplets out in the marketplace. And we drove that extension to the JEP30, the PartModel, back in January of 2023. That is now a JEDEC standard.

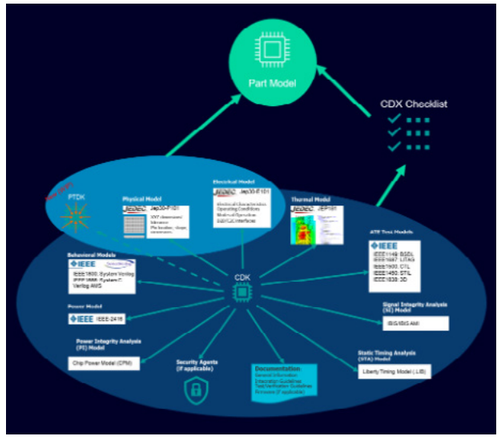


Figure 2: Chiplet design kit (CDK): JEDEC JEP30 PartModel.

We next developed checklists for other formats and recommended the models required to support design analysis. At a minimum, we have a checklist to know what models are available. A chiplet designer or chiplet provider can define which models are available. There are also provisions where we can include the models, and that's really up to the chiplet provider if they want to include that in the part model.

Package Assembly Design Kits

Today, we are actively working on the package assembly design kits. These include the rules for defining pitch, spacing, and the type of connectivity components used to connect the chiplets to the interposers and substrate.

In keeping with our guidelines, they are in a machine-readable format, and they are EDA-neutral. Thus, each of the EDA vendors, assuming they're supporting these formats, would be able to take those rules from a single source. This results in much cleaner access for the FABs and the OSATs during manufacturing, because they can provide these rules in one format that all the EDA tool vendors can use. With access to this information and these machine models, the PADKs can be used for scripting directly in some of the EDA tools.

Material Design Kits

Another area we are working on is material design kits. These are a truly novel idea. When engineers are doing analysis—whether it be thermal, stress, signal integrity, or power integrity—the MDKs can define the material properties that are in the package components inside the package. Again, the idea is to put these in a machine-readable format, rather than having that information derived ad-hoc from the vendors and material providers and manually input into the tools. Then the tools would use the MDKs to use that material information directly for analysis.

Package Test Design Kits

As the name implies, package test design kits are for test. The chiplet model contains a lot of information in terms of the physical dimensions of the device, also the pins, and the functional mode. But when you're testing these devices, typically there is a different set of pins that are used to test for wafer sort when you're testing the wafers. The PTDKs define the location of those pins, the modes, the physical location, the shapes, and all the geometries.

Workflows to Support 3D IC

Another benefit of a PartModel, and one of its targeted purposes, is to enable a chiplet market ecosystem. Chiplet suppliers can design a chiplet, and if they want to offer that to the market, they can describe all the required information and make it available.

This gives chiplet suppliers the ability to define essentially the information about their products in an electronic catalog, in which designers can see the different available parts and choose the ones best suited for their particular design.

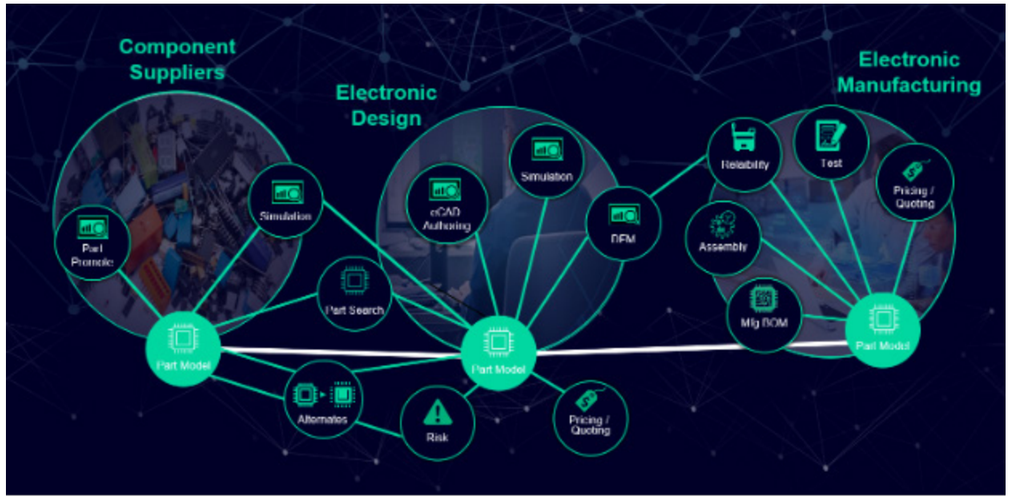


Figure 3: Bridging the chasm in the electronics value chain.

Thus, chiplet providers can empower prospective customers to search for their chiplet IP and assess functionality, detailed electrical/physical attributes, and available design models. System designers and chiplet consumers can then look through that catalog and also do business transactions. Finally, the 3DK models can be used for the design and verification process, and eventually handed off to manufacturing.

Lastly, we are advancing the development of the authoring tools required to create these models. The 3DK models are in CDX format, and this is not a friendly format for someone to type, so there is a need for an open-source EDA-neutral authoring tool. The goal is to have a single tool that will create each of these 3DK models, and the specific EDA vendors, manufacturers, and assemblers would then use the EDA-specific implementations to create the decks, etc. Toward that end, Siemens EDA introduced Innovator3D IC. Innovator3D IC offers a comprehensive multi-physics cockpit for 3D IC design, verification, and manufacturing to deliver a fast, predictable path for the planning and heterogeneous integration of ASICs and chiplets.

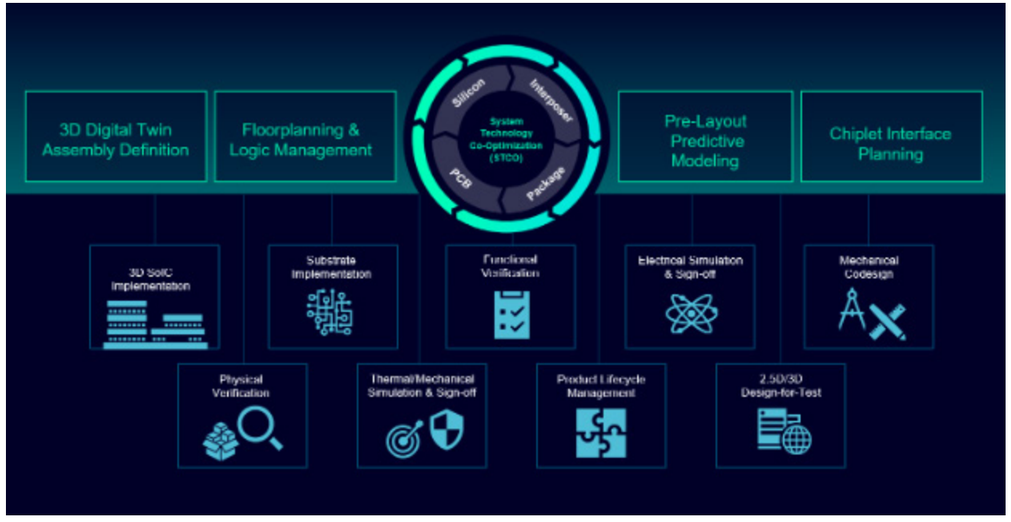


Figure 4: The Innovator3D IC - heterogeneous integration cockpit.

As this article has attempted to show, the CDX working group has been hard at work to provide the open source, EDA neutral, machine-readable 3DKs and chiplet authoring tools that will propel 3D IC heterogeneous integration into the mainstream of electronic systems design. And we'll be coming to your town very soon.

Hot Spots in Advanced Packaging Around the Globe

For those of you who recognize the double entendre in the title and question the focus of this year's cover feature, let me assure you: It's not about thermal management solutions for next-generation advanced packaging. It is about the rising importance of advanced packaging and the activities that it's stimulating around the globe.

For decades, semiconductor packaging was nothing more than a necessary step to ensure the connection and protection of semiconductor chips on the circuit board and nothing more. Because it was a cost adder, the industry goal was to do it as cheaply as possible. Most semiconductor manufacturers in the U.S., Asia, and Europe shipped their packaging offshore.

As Moore's Law slows, heterogeneous integration approaches using advanced packaging technologies are now critical to ensuring the power, performance, area, and cost requirements for today's leading-edge processors. This fact is changing the global importance of advanced packaging, which has become a value-add to system-level performance.

Five years ago, when the COVID pandemic created a global chip shortage, governments worldwide recognized how critical semiconductors are to our everyday lives. Simultaneously, geopolitical tensions increased and artificial intelligence applications demanded advanced AI chipsets.

This increased concern about the impact semiconductors have on national security. As a result, we saw increased investments from Europe, Asia, and the U.S. to build regional ecosystems for onshoring semiconductor manufacturing.

Many say that 2024 will go down in history as the Year of Advanced Packaging. As regions around the world compete for semiconductor manufacturing market share, they are all investing in advanced packaging R&D. Centers of excellence are popping up everywhere.

This issue of the 3D InCites Yearbook takes a deep dive into global advanced packaging activities in Europe, Asia, and North America, with a special focus on activities in Arizona. Read on!

How Arizona is Growing its Advanced Packaging Capabilities

An inside look at how ASU, local governments, and private sector companies are working together to make Arizona a hub for advanced packaging innovation.

By Jillian McNichol

The year 2022 was monumental for the semiconductor industry. That year, the Biden-Harris administration committed to making the U.S. a world leader in semiconductor manufacturing by passing the bipartisan CHIPS and Science Act. In an effort to decrease the nation's reliance on China for chips, and to meet the demands of advanced technologies, the CHIPS Act highlighted plans to invest $53 billion in onshoring semiconductor manufacturing, with $1.6 billion going toward advanced packaging. (Figure 1)

Figure 1: YES is just one advanced packaging company investing in Arizona. Vic Chaudhry, VP and head of stragic marketing hosted Jillian McNichol at the YES facility in Chandler, AZ.

Due to current onshoring efforts for semiconductor manufacturing, it wouldn't make sense to build front-end capacity in the U.S. only to send the chips overseas to be packaged. With a major boost in funding pouring into the country's advanced packaging ecosystem, it's almost hard to believe that packaging was once regarded as little more than a cost burden. In a swift change of events, it's emerging as the industry's best chance for continuing Moore's Law. This famous industry observation states that transistors on an integrated circuit (IC) will double every two years.

To keep up with power, performance, area, and cost requirements, the industry is turning to advanced packaging technologies like 2.5D and 3D stacking. By optimizing the package, chip manufacturers can continue to pack more compute power in less space. This is essential for advancing artificial intelligence (AI), high-performance computing (HPC), and more.

As advanced packaging moves into the spotlight, Arizona is becoming a key player in this integral manufacturing process. As a result, local governments and private sector companies are collaborating to boost Arizona's semiconductor manufacturing dominance.

Arizona's Private Sector Growth

In February 2024, Amkor announced the approval of its outsourced semiconductor assembly and test (OSAT) facility in Peoria, Arizona. Once the facility is completed, it will make history as the largest OSAT facility of its kind in the U.S. (Figure 2)

Figure 2: Rendering of the future Amkor Technologies Facility in Peoria, AZ

Amkor's $2 billion investment will not only provide Arizona with a world-class packaging center, but it will also create 2,000 new jobs for Arizonans. In addition, Amkor is the only U.S. headquartered OSAT provider that offers both high-volume manufacturing and advanced packaging capabilities. Although the facility's opening date has yet to be announced, its creation marks a leap forward in strengthening Arizona's advanced packaging foothold.

Alongside its new facility, Amkor also announced a memorandum of understanding with TSMC to work together on delivering high-volume advanced packaging and testing technologies to its customers. The proximity of Amkor's upcoming back-end facility and TSMC's front-end fab will help further improve product cycle times, boosting industry activity in the Valley.

While I was interviewing companies for this article, I asked all of them why they chose to have a presence in Arizona. I received several answers, but access to government funding, proximity to local and California-based customers, and a robust talent pipeline came out on top. However, something I found particularly interesting was learning just how purposeful Arizona's move into advanced packaging has been.

"You have everybody from the governor down focused on growing a semiconductor ecosystem," said Eelco Bergman, Chief Business Officer at Sara's Micro Devices. Sara's Micro Devices opened its first Arizona manufacturing center in Chandler in January 2024. (Figure 3)

Figure 3: Eelco Bergman, Chief Business Officer at Sara's Micro Devices, hosted a visit with Jillian McNichol.

Bergman shared that Arizona's governmental organizations, such as the Arizona Commerce Authority (ACA), the Greater Phoenix Economic Council (GPEC), and city governments, are focused on attracting semiconductor companies. This strong government support, as well as competition between cities, helps bring the talent needed to create a thriving ecosystem.

“None of these companies, including ourselves, operate on their own,” Bergman said.

Similar to Sara's Micro Devices, Yield Engineering Systems (YES) also opened a new facility in Chandler in July of 2023. Incidentally, the two companies share the building. (Figure 4)

Figure 4: YES and Saras share their home in Chandler, AZ.

Vik Chaudhry, VP and Head of Strategic Marketing at YES, mentioned that the company opened its new facility in Chandler to be close to two of its biggest customers - Intel and TSMC. The city’s large talent pool and business-friendly climate also drew YES in.

The company has a strong focus on glass core substrates, and with the continued growth in this area of packaging, the company expects to add around 100 new roles in the foreseeable future.

Arizona State University’s Role in the State’s Semiconductor Ecosystem

With so much emerging innovation in Arizona, the state needs to build and retain a robust and talented workforce. Although workforce development has historically been a hurdle for the semiconductor industry, Arizona State University (ASU) is helping to bridge this gap.

"We have a close relationship with not just the city and the state, but also with ASU," said Ron Huemoeller, CEO of Sara's Micro Devices. "ASU has a significant amount of funding and effort going into package development that we are now a part of with them. There's a big assist with development and talent, and they also help us with access to the government."

But ASU isn’t the only university in the U.S. that has semiconductor initiatives. Earlier this year, Northern Arizona University received a $13 million grant from the ACA to fund its semiconductor metrology program. The University of Arizona also has a Center for Semiconductor Manufacturing, where students can earn a graduate certificate in microelectronics packaging. Additionally, the Maricopa County Community College District introduced a 10-day training program for semiconductor technicians.

So I had to ask—what sets ASU apart from other schools across the country? From what I gathered, other schools also have stellar research capabilities, but they're not located in states where growing the advanced packaging industry at large is a top priority. To learn more about ASU's role in expanding advanced packaging, I visited ASU's MacroTechnology Works center in Chandler. While I was there, I spoke with key leaders from both ASU and Deca Technologies.

In March of 2024, the two organizations announced their partnership to create North America's first Fan-Out Wafer-Level Packaging (FOWLP) research and development capability. FOWLP is a packaging approach that helps build higher-density packages by fanning out the interconnects through a redistribution layer (RDL), and it does this at a lower cost than silicon interposer technology. FOWLP is important because high-density packages are becoming increasingly relevant for scaling AI, electric vehicles, and more.

The Relationship Between ASU, Deca, and the State of Arizona

Although the R&D center is still in progress, the partnership between ASU and Deca is very much alive. For instance, this past November, the National Institute of Standards and Technology (NIST) announced that ASU and Deca were selected to lead the SHIELD USA initiative. This project aims to promote innovation within the domestic advanced packaging industry, expand capacity, and help the U.S. regain its leadership in this area of microelectronics.

With so much in the works, I asked Zachary Holman, Vice Dean for Research and Innovation for ASU’s Ira A. Fulton Schools of Engineering, about how the ASU and Deca partnership came to be.

In short, Holman shared that federal and state funding allowed ASU and Deca to form their partnership. Deca is a leading provider of advanced packaging technologies headquartered in Arizona, and the company is most known for high-volume FOWLP solutions that power many of the world's smartphones. In addition, ASU's Fulton Schools of Engineering had 33,000 students as of 2024.

However, ASU wasn’t always strong in packaging, so I had to ask. What made ASU want to compete in this industry? Was this driven by the state’s increasing need for packaging talent? The short answer is yes.

Holman highlighted that in 2020, ASU began working on its strategy for microelectronics in terms of university research, partnership, and innovation. He mentioned that ASU initially focused on materials due to its existing expertise in that area. The university soon expanded into advanced packaging to meet the needs of the local semiconductor ecosystem.

"We realized that we needed to produce the talent for these companies to hire and that we needed to have innovative faculty members who were teaching that next generation," Holman said. "So, we made a strategic play in packaging."

Holman also shared that Deca was a natural partner due to its proximity to ASU, and he emphasized Deca’s advanced technology and natural understanding of ASU’s goals. It was easy to find common ground, he said, because the company had a strong grasp on the future of advanced packaging.

Together, the organizations work to attract talent and align their efforts to meet the demands of Arizona’s advanced packaging needs. Tim Olson, CEO of Deca, echoed the benefits of this partnership.

"We needed a partnership where we could have a physical facility and continue to innovate - to take what we had and continue to build future generations," said Olson. "ASU is perfect for that. Perfect location-wise, perfect mindset-wise."

A big part of teaching the next generation of packaging professionals is providing them with hands-on experience. While I was at MacroTechnology Works, I asked Holman to explain the difference between gaining real-world experience at ASU and gaining experience as an intern in a fab (Figure 5).

Figure 5: The lobby at ASU’s MacroTechnology Works. The cleanroom space is shared by ASU, Deca, EV Group, and Applied Materials.

"As an intern, you don't get to go into the fab and turn a knob, because you might break something," he said. "Internships are fantastic for students, but someone that is on a three-month summer internship isn't going to have responsibility."

With students gaining direct, hands-on experience with advanced packaging tools, Holman also shared advice for companies that want to engage students earlier on.

Students, he said, are using equipment that was donated by local companies, and those companies have engineers who come to ASU and explain how the tools are used in fabs. This approach helps turn students into ambassadors for the tool companies because they've worked on their systems before. Students may also end up working at the tool companies themselves.

Perspective From Long-Established Arizona Semiconductor Companies

As The CHIPS Act and local government funds made its way into the state, I wanted to know how recent growth impacted semiconductor companies that were already in Arizona. Did they benefit from any of this, or were they too far ahead of their time?

To find out, I revisited the MacroTechnology Works facility to meet with EV Group—a company that has been in Arizona since 1994. EV Group is headquartered in Austria and has a broad global presence, but its Chandler facility is home to a class 100 cleanroom and onsite equipment lab (Figure 6). While I was there, I spoke with Vineeth Reddy Bijjam, the company’s Director of Technology and IP.

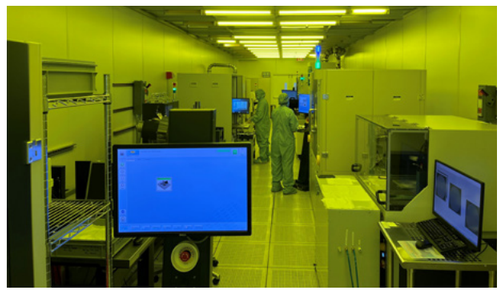


Figure 6: A peek inside EV Group’s Class 100 clean room located in MacroTechnology Works.

Right from the beginning, EV Group's founders believed that Arizona would become an epicenter for semiconductor technology. Although the company didn't receive state or federal funding, Bijjam shared that EV Group benefits from local growth indirectly because its customers are now incentivized to come to the state.

"Our lab is a strategic piece of infrastructure that's helping us partner with local customers," said Bijjam. "We engage with them in the very early stages of development and provide them with a shorter feedback loop, so they don't have to wait for broader lead times to get their prototypes."

In addition to customer partnerships, Bijjam also highlighted EV Group's active internship program with ASU and the company's relationship with several university professors.

Finetech is another global company with a longstanding Arizona location. Opened in 1999, Finetech's Mesa, Arizona location is home to its sales and support center for all equipment it sells in the U.S. The Mesa location also features a showcase room with all of the company's equipment, so customers can run feasibility trials and access Finetech's process development services. (Figure 7)

Figure 7: EV Group's Vineeth Reddy Bijjam, Director of Technology and IP, hosted Jillian McNichol's visit.

"University sales have really picked up in the past year, specifically due to funding from the CHIPS Act," said Neil O'Brien, General Manager at Finetech Americas.

O'Brien also highlighted increasing opportunities for Finetech to work with customers on process development and experimentation initiatives, specifically on projects that have received funding from the CHIPS Act.

Key Takeaways

Arizona is working to create a robust advanced packaging ecosystem, with all parties working effectively together to build the future of this industry. Local governments are incentivizing businesses to bring their advanced packaging capabilities to Arizona, and ASU is working to educate and train the next generation of packaging professionals in accordance with the needs of Arizona's local companies.

Although companies that had a pre-existing presence in Arizona aren't benefiting from funding directly, the influx of new businesses in the state has led to increased tool sales, partnership opportunities, and access to a broader talent pool.

Will Arizona be able to maintain its momentum and establish itself as a North American hub for packaging innovation? Only time will tell, but I'm optimistic for the future.

2024: A Year of Growth and Innovation

By Peter Dijkstra

2024 was another year of significant growth for Trymax Semiconductor Equipment B.V. This year was marked by several pivotal developments, including the successful ramp-up of our new manufacturing facility, the establishment of a dedicated quality department, the expansion of our team with additional Field Service Engineers, and the growing momentum of our USA team, which resulted in multiple purchase orders.

In the broader market, while the automotive sector remains stable, particularly in silicon carbide (SiC) applications, other markets have experienced slower growth. However, we have observed a substantial increase in the storage and availability of data, with ambitious forecasts driven by the increasing demand for high-speed data access everywhere.

The most substantial growth for Trymax this year came from advanced packaging applications. Our process team has been dedicated to developing various process applications related to 2D, 2.5D, and 3D packaging technologies. In 2D IC packaging, components are arranged on a single plane. In 2.5D IC packaging, components remain on the same plane, but an interposer allows for additional integration. 3D IC packaging involves vertically stacking components, enabling higher levels of integration and potentially improved performance and power efficiency. These devices are increasingly interconnected using through-silicon vias, which are fabricated using the Bosch process.

Our Trymax Process Module excels at efficiently cleaning residual polymer after the Bosch process. Additionally, to facilitate easier copper filling of the created vias, our Process Module is capable of creating a bowl etch on top of the vias.

Before Chip-to-Wafer (C2W) or Wafer-to-Wafer (W2W) stacking, it is essential to clean and, where possible, activate surfaces. Our Trymax low-cost Process Module simplifies this cleaning process while simultaneously activating the surface to make it more hydrophilic.

On behalf of the entire Trymax team, I would like to extend our heartfelt thanks to our customers and suppliers for the trust and confidence they have placed in us throughout this year.

Empowering the Future: New York's Semiconductor Surge in 2024

By Scott Sikorski, Ph.D., IBM

In 2024, New York's semiconductor industry experienced substantial growth, driven by increased funding from both the U.S. government and the expansion of IBM along with other key industry suppliers. As a result of these recent public and private initiatives, the NY CREATES' Albany NanoTech Complex—the largest non-profit semiconductor R&D facility of its kind in the nation—is expanding in size and capabilities.

This state-of-the-art facility has been instrumental for over two decades in fostering advancements in chip technology through collaboration among industry leaders, academic institutions, and international partners. The growth of the semiconductor sector in New York and throughout what is now referred to as the Northeast Corridor has been evident, with numerous announcements throughout 2024. Below is a summary of a portion of 2024's news from the region.

Key 2024 New York Semiconductor Developments:

IBM Quantum System One Launch

In April, Rensselaer Polytechnic Institute (RPI) and IBM unveiled the world's first IBM Quantum System One located on a university campus. This groundbreaking installation aims to enhance quantum computing research, workforce development, and educational initiatives in New York, further solidifying the partnership between RPI and IBM.

ASMPT and IBM Partnership Renewal

In July, ASMPT and IBM renewed their collaboration to advance chiplet packaging technologies. This partnership focuses on enhancing thermocompression and hybrid bonding techniques for chiplet packages, utilizing ASMPT's advanced Firebird TCB and Lithobolt hybrid bonding tools. This renewed effort builds on previous developments in hybrid bonding, aiming to create lighter, faster, and more energy-efficient semiconductor packaging solutions.

Investing in Next-Gen Chips Research

As part of the FY 2025 budget, New York State Governor Kathy Hochul secured a $500 million capital investment for NY CREATES' Albany NanoTech Complex to jumpstart a $10 billion partnership and bring a cutting-edge High NA EUV Lithography Center to the complex.

IBM Expansion at NY CREATES' Albany NanoTech Complex

In September, IBM announced plans to lease an additional 30,000 square feet at the Albany NanoTech Complex. This expansion is designed to accommodate a significant increase in the workforce, with plans to grow from 700 employees to between 850 and 999. The new agreement allows IBM to lease space in the ZEN building, which offers a total of 365,000 square feet, already fully occupied by IBM on its top floor.

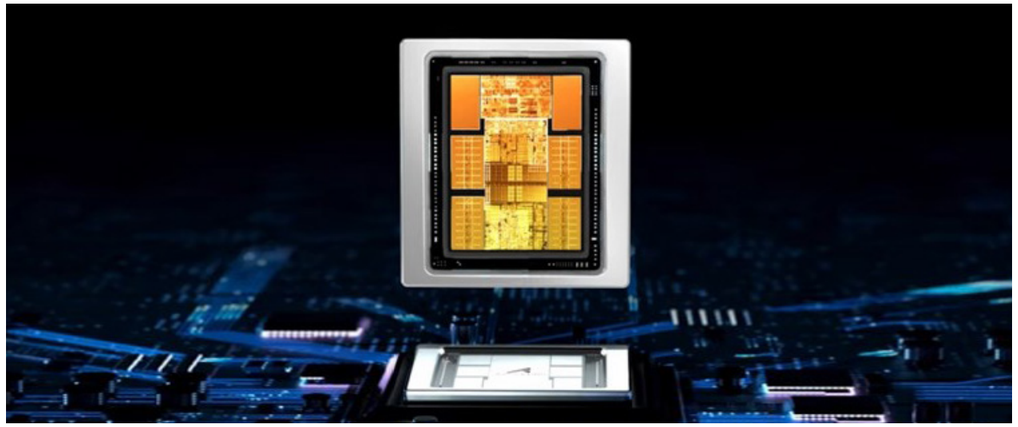
Federal Funding for NORDTECH

Also in September, Governor Hochul celebrated the award of over $30 million from the U.S. Department of Defense to support the NORDTECH research teams. This funding establishes the Northeast as a Department of Defense Innovation Hub and is intended to stimulate the development of a domestic microelectronics manufacturing industry. NORDTECH, formed in September 2023, is a regional coalition that includes key institutions like NY CREATES, the University at Albany, Cornell University, RPI, and IBM, all focused on creating a pathway from research ("lab") to production ("fab").

NSF Grant for Workforce Development

On September 30, NY CREATES announced it received a $4.7 million grant from the National Science Foundation to launch a Semiconductor Workforce Development Program. Senate Majority Leader Charles Schumer emphasized that this funding, part of the CHIPS & Science Act will provide college students nationwide with hands-on training at Albany NanoTech, preparing them for careers in the semiconductor industry.

Overall, these initiatives highlight New York's strategic position as a key player in the semiconductor landscape, driving innovation and workforce development in this critical field. IBM is proud to play a crucial role in this growth, supported by our world-class labs and manufacturing facilities in Albany, Yorktown Heights, the mid-Hudson Valley, and other parts of the thriving Northeast Corridor.



(Source: Nvidia)

Asia May Still Be the Hottest Spot for Advanced Packaging

By Dean Freeman, Freeman Technology and Market Advisors

When the United States and Europe looked to reshore semiconductor technology, the primary focus was restoring leading-edge manufacturing and creating more resilient supply chains throughout the ecosystem. Eventually, it emerged that nearly all of the leading-edge packaging took place overseas, and there was minimal packaging capability in either the U.S. or Europe.

This should not come as a surprise to anyone involved in the industry. Almost as soon as the semiconductor industry started manufacturing chips; test, assembly, and packaging were moved offshore, as it was considered more economical to perform those tasks overseas. This trend led to strong growth of outsourced semiconductor assembly and test service (OSATs) providers and integrated device manufacturer (IDM) packaging across the Asia Pacific (AP) region.

The Asia Times wrote that advanced packaging is the next front in the chip wars. If you think that conquest or success in war arises from how much territory, or in this case manufacturing is performed in Asia, then this will be a long-drawn-out battle where the Asia Pacific region already has most of the territory. When the U.S. Department of Commerce (DOC) was preparing the arguments for the CHIPS Act, it was determined that only 3% of the packaging occurred in the U.S., and of that very little advanced packaging when the report was first written.

While the U.S. is attempting to recover some of that packaging share, the real hotspot for packaging is in the Asia Pacific Region. The market can be broken up into the semiconductor fabs that also do advanced packaging either for themselves or foundry partners and the OSAT companies, which are essentially the packaging and test foundries for the majority of the industry. SEMI is tracking over 500 OSAT providers and 170 IDM facilities. As the graph shows the majority of these packaging facilities are in the Asia Pacific region.

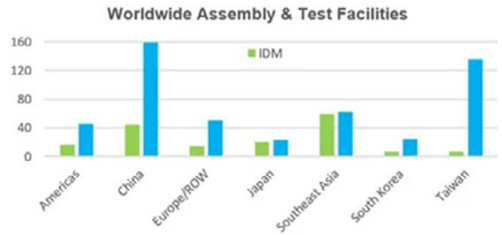


Figure 1: Worldwide Assembly and Test Facilities (Source: SEMI)

Companies manufacturing chips, both IDM and foundry, provide a considerable amount of packaging services in the AP region. The foundry operations of Samsung and TSMC have significant packaging capacity and are adding more as demand for chiplets to support AI capacity for their partners. Chiplets are also finding their way into phones, automotive, and PCs, which is increasing the demand for chiplet capacity to which the OSATs are responding in partnership with fabs and foundries.

Samsung, Hynix, and Micron perform most of their memory packaging in the AP region. Samsung and Hynix are packaging mostly in Korea with some manufacturing occurring in China. Micron has facilities in Singapore, Malaysia, China, and Taiwan. Micron is also expanding to India with a new facility expected to open in 2025. Intel has packaging and assembly facilities in Malaysia, China, and Vietnam in addition to its U.S. efforts.

OSATs makes up the bulk of the packaging resources for the semiconductor industry. Most of these facilities are located in the AP region, with China and Taiwan having over half of the OSAT facilities and revenue across the industry. According to IDC, the top 10 OSAT companies are responsible for over 80% of the industry's revenue, with ASE and Amkor, the top 2 OSAT companies, accounting for over 40% market share. The top 10 OSATs are located primarily in Taiwan and China, with one in Singapore. The OSATs have facilities spread throughout the AP region, for example, Amkor has packaging facilities in Taiwan, China, Korea, Japan, Malaysia, Vietnam, and the Philippines.

1. **ASE Group:** Headquarters Taiwan
2. **Amkor:** Headquarters U.S., Manufacturing mostly AP
3. **Powertech Technology Inc:** Headquarters Taiwan
4. **Chipmos Technologies:** Headquarters Taiwan
5. **King Yuan Electronics Co. Ltd:** Headquarters Taiwan
6. **Formosa Advanced Technologies:** Headquarters Taiwan
7. **JCET:** Headquarters China
8. **UTAC Holdings Ltd:** Headquarters Singapore
9. **Lingsen Precision Industries Ltd:** Headquarters Taiwan
10. **Tongfu Microelectronics Co.:** Headquarters China

Figure 2: Worldwide Top 10 OSAT companies, 2024 market share. (Source: IDC)

With all of the chiplet noise in the marketplace, one might think that most of the chiplet development occurs either at TSMC in Taiwan or at Intel in the U.S. This is far from the case. A considerable amount of chiplet devices are assembled and packaged at the OSATs. AMD has partnered with Tongfu Micro to handle its chiplet packaging. Tongfu and AMD co-developed their chiplet capability in 2017 when AMD first started chiplet development. Intel's Embedded Multi-die Interconnect Bridge (EMIB) packaging, which is considered 2.5D, is done in Malaysia as well. Foveros is packaged in the U.S. at the moment, but that may also be outsourced to AP.

Samsung has a considerable 3D packaging effort for its advanced logic foundry partners, Samsung Advanced Logic, and HBM located in Korea. SK Hynix performs most of its HBM packaging and development in Korea as well. All the memory companies are partnering with TSMC, or other OSATs to get their HBM integrated into advanced packages.

OSATs are a big part of the 3D ecosystem, an most packaging development happens at these companies. ASE has long partnered with TSMC and got a shout-out at TSMC's North America OIP presentations. Amkor is also moving forward with TSMC in Arizona for 3D packaging technology.

Panel-level packaging (PLP) is a hot new technology for chiplet manufacturing. Wafer-level packaging (WLP) cannot support the volume of chiplet devices needed by the microelectronics industry. The industry is shifting from using wafers or round substrates to glass panels. Innolux in Taiwan is operating a 3.5G panel-level packaging plant. TSMC just purchased a 5.5G flat panel factory for the same purpose and Micron has been looking at several flat panel facilities for PLP. TSMC expects to have a 9-reticle package in production by 2027.

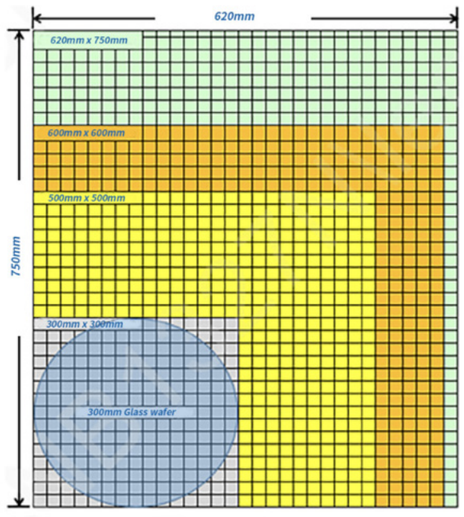


Figure 3: Panel level packaging panel dimensions (Source: Innolux)

Advanced packaging will continue to be an area of strong growth for the industry. In a recent earnings call, CC Wei, CEO of TSMC, mentioned that in 2023, the foundry business was about $117 billion; however, with the addition of advanced packaging to TSMC's and other companies' product lines, the foundry business was estimated to be 250 billion dollars. That's a doubling of the foundry market and is mostly due to advanced packaging.

With a market size of over $100 billion and no signs of the AP region slowing down in the packaging market, AP will continue to be the hot spot for advanced packaging for some time to come.

US-JOINT Consortium: Strengthening Advanced Packaging Innovation Across Borders

By Avery Gerber

As global semiconductor demand continues to surge, international collaboration has become essential for driving technological innovation. The US-JOINT consortium represents a key initiative in fostering cross-border cooperation between Japan and the United States. This groundbreaking collaboration brings together 10 companies- Azimuth Industrial Co. Inc., KLA Corp., Kulicke & Soffa Industries Inc., TOWA Corp., ULVAC Inc., Moses Lake Industries Inc., MEC Co. Ltd., NAMICS Corp., Tokyo Ohka Kogyo Co. Ltd., and Resonac Corp. to work on advanced semiconductor packaging research and development. Three of these companies—**KNS, NAMICS, and KLA**—are members of the 3D InCites community.

In response to the growing need for sophisticated packaging solutions, the US-JOINT consortium aims to leverage the unique strengths of its participants in both countries. I spoke with several key members, including Kazuyuki Mitsukura, the technical director leading US-JOINT at Resonac America, to learn more about the initiative's goals. We also spoke with representatives from KLA, Kulicke & Soffa, and NAMICS.

"US-JOINT is being established with the participation of 10 companies, including U.S.-based firms," Mitsukura said. "This program builds on the experience of JOINT2, facilitating collaboration with participants and customers from major semiconductor, fabless, and tech companies. We are setting up US-JOINT in Silicon Valley, where cutting-edge semiconductor designs are born."

He highlighted a paradigm shift in semiconductor development. "It's no longer just about front-end processes; packaging processes are now equally important to achieve the performance required for modern applications. The growing influence of companies like Google, Amazon, and other tech giants in the semiconductor industry highlights the need for a holistic approach that integrates both design and packaging to drive innovation," Mitsukura added.

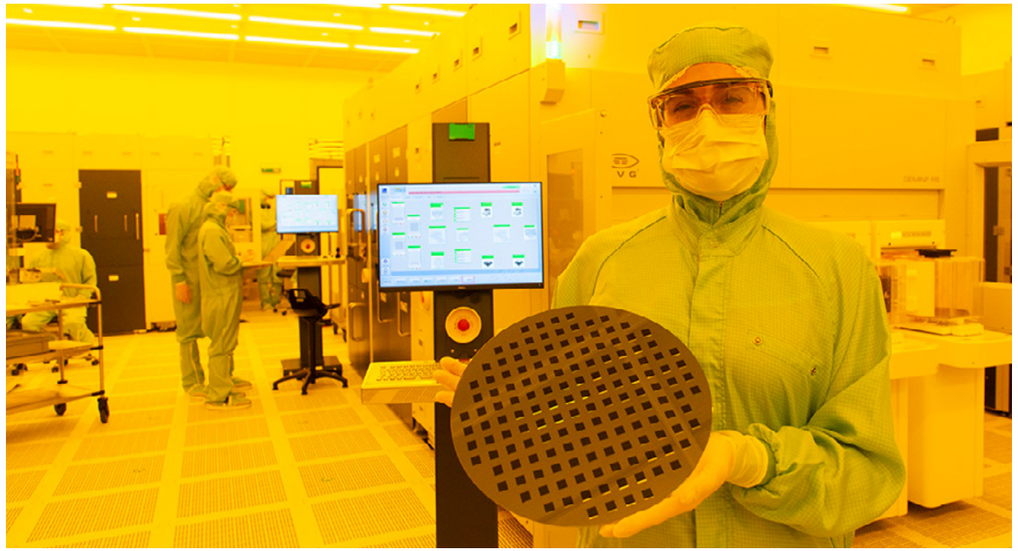
Ken Araujo, Vice President of Sales and Marketing at NAMICS, emphasized the strategic advantage the US-JOINT consortium provides in introducing next-generation materials for advanced packaging solutions.

"This initiative allows us to showcase new materials directly to customers who may have emerging 3D or complex package designs," Araujo said. "By using the consortium's resources, we can conduct real-world evaluations rather than relying on simulations. This helps customers understand if materials, such as underfill or liquid compression molding (LCM), are compatible with their designs, while also providing us with immediate feedback."

Araujo also noted that the hands-on collaboration at US-JOINT would not only reduce design cycles but also help NAMICS fine-tune its material development to align with evolving customer needs.

"Instead of using test vehicles or purely simulation-based studies, we can build actual products at the consortium. This allows us and our customers to see firsthand if these materials work within their intended packages or if design modifications are required," Araujo added.

Continued on page 69



Navigating the European Chip Renaissance

By Paul Lindner, EV Group

Governments around the world are increasingly recognizing the strategic importance of semiconductors to national security as well as in fueling innovation in many industry sectors. As a result, nations are investing billions of dollars to expand semiconductor manufacturing and packaging infrastructure on their shores.

For example, the U.S. CHIPS and Science Act, which was signed into law two years ago, aims to invest $280 billion in new funding to boost domestic research and development semiconductors, of which nearly $53 billion in subsidies has been allocated for semiconductor manufacturing. Across the Atlantic, the European Chips Act will invest more than €43 billion ($47 billion) through 2030 to bolster Europe's competitiveness and resilience in semiconductor technologies and applications and help achieve both the digital and green transition. Other nations, including China, Japan, Korea, Taiwan, and India, have announced their plans to invest billions in semiconductor subsidies.

While much attention has been centered on building leading-edge semiconductor fabs for making the most advanced memory and logic devices, strategic investments are also being made in building the infrastructure and supply chains for heterogeneous integration technologies. These include investments in advanced packaging, MEMS and sensors, power devices, and photonics—all of which play a vital role in driving semiconductor innovation.

Europe has historically played and continues to play a crucial role in driving semiconductor innovation and device scaling through core strengths across the semiconductor value chain. These strengths include semiconductor design software, advanced materials development, critical manufacturing processes such as lithography and wafer and die bonding, device manufacturing such as sensors and power devices, advanced packaging, as well as beyond-CMOS technologies such as photonics and optical computing as well as quantum computing.

This article will review several major investment activities by the European Union that are driving a new "European chip renaissance" and strengthening the region's semiconductor and micro-electronics infrastructure. This article will also review recent examples of partnerships between EV Group and manufacturers, research institutes, and other key players in Europe to enhance Europe's competitiveness and leadership in advanced technology.

The Path to Revitalization

Europe has historically been a leader in semiconductor research and development, as well as in manufacturing equipment. CEA-Leti, Fraunhofer, imec, and myriad other institutes and universities have led the charge in discovering and developing new technologies that have enabled new levels of innovation in semiconductor manufacturing and packaging.

ASML, one of the largest semiconductor equipment companies, is the only manufacturer of EUV lithography systems, which are needed for the most advanced design nodes. EV Group and Besi are leaders in wafer-to-wafer and die-to-wafer bonding, respectively, which are essential process technologies for enabling 3D/heterogeneous integration. ARM, Soitec, Carl Zeiss, and

many other industry-leading companies, universities, and research institutes headquartered in Europe round out the supply chain from design IP, materials, and critical components needed for semiconductor manufacturing.

Europe has also been a historic leader in semiconductor and micro-electronics device manufacturing, particularly in the areas of MEMS and sensors, power devices, and microcontrollers for the consumer electronics, industrial, and automotive markets thanks to Infineon, NXP Semiconductors, STMicroelectronics, and numerous others. However, despite holding about a quarter of the world's semiconductor production 25 years ago, Europe represents less than 10% of global semiconductor production today, making the region particularly vulnerable to supply chain disruptions and geopolitical challenges. To reverse this trend and bolster Europe's competitiveness and resilience in semiconductor technologies and applications, the European Union approved the European Chips Act (ECA) in July 2023, aiming to mobilize more than €43 billion in investments by 2030. The goal is to double Europe's global manufacturing market share from 10% to 20% by 2030.

In November 2023, the European Commission launched the Chips Joint Undertaking (Chips JU) under the ECA. As part of its charter[1] the Chips JU will:

- Set up pre-commercial, innovative pilot lines, providing industry state-of-the-art facilities to test, experiment, and validate semiconductor technologies and system design concepts, as well as provide for small-scale production
- Deploy a cloud-based design platform for design companies across the EU
- Support the development of advanced technology and engineering capacities for quantum chip
- Establish a network of competence centers and promote skills development

The pilot lines are a critical component of this effort, serving as a platform for European research and development with an industrial perspective to bridge the gap from lab to fab. In April 2024, the Chips JU completed its evaluation of various pilot line proposals that had been submitted to the group, and selected four proposals that have been approved by the EU and are starting now:

- **NanoIC:** sub-2-nm system-on-chip pilot line; hosted by imec; focusing on advanced logic, memory and interconnect technologies such as gate-all-around nanosheets, CFETs, high-NA EUV lithography, spin-orbit torque magneto-resistive random-access memory (SOT-MRAM) architectures, 3D electrical interconnects for scaled-pitch die-to-wafer (D2W) hybrid bonding and high-density redistribution layer technologies, and optical interconnects for D2W hybrid bonding[2] (Figure 1).

Figure 1: Imec's headquarters campus features semiconductor cleanrooms and state-of-the-art labs. Shown here is the imec tower and cleanroom. ©imec.

- **FAMES:** fully depleted SOI pilot line; coordinated by CEA-Leti; focusing on FD-SOI (with two new generation nodes at 10nm and 7nm), embedded non-volatile memories (OxRAM, FeRAM, MRAM, and FeFETs), radio-frequency components (switches, filters and capacitors), 3D heterogeneous integration and sequential integration, and small inductors to develop DC-DC converters for power management ICs[3]. (Figure 2)

Figure 2: For nearly six decades, CEA-Leti has been pioneering innovation in micro- and nano-technologies. Shown here is Leti's facilities in Grenoble, France. ©Pierre Jayet.

- **AHSI:** advanced heterogeneous system integration pilot line; led by Fraunhofer; focused on the development of advanced packaging and integration technologies that combine various semiconductor materials, circuits, or components into a single compact system—utilizing innovative techniques like System-in-Package (SiP) and 2.5D/3D integration to enhance the performance and functionality of semiconductor devices.[4]
- **WBG:** wide bandgap pilot line; coordinated by Italy's National Council of Research; to be built in Catania, Italy; focusing on materials such as silicon carbide (SiC) and gallium nitride (GaN) that allow electronic devices to operate safely at much higher voltage, frequency, and temperature than standard silicon-based counterparts with unmatched efficiency gains for developing highly efficient power systems in electric vehicles, lighter-weight electronics, and radio-frequency equipment.[5]

Several new rounds of calls for proposals have been issued in 2024, including:

- A proposal for a pilot line on advanced photonic ICs, which are expected to be critical for next-generation high-performance computers, high-speed communications, and data centers. This call for proposals recently closed in September 2024.
- A proposal for the creation of "competence centers" to provide access to technical expertise and experimentation in semiconductors, something that some equipment companies such as EV Group have already implemented for their customers and partners. This call for proposals recently closed in October 2024.
- A proposal for the creation of a cloud-based online design platform that will allow users, particularly academia, start-ups, and SMEs, to design and develop their new chips, and to help bring their designs to market.
- Several proposals to fund pilot lines for quantum chips focused on stability and trapped ions, respectively, targeting applications such as solving complex optimization problems in logistics and supply chain management, accelerating drug discovery through molecular simulations, enhancing cybersecurity with advanced encryption methods, and improving artificial intelligence and machine learning algorithms.[6]

Bringing Triple-i to the European Chips Act

Through bold action, the EU has undertaken an ambitious journey to reinvigorate the European semiconductor industry and bring about a new "chip renaissance." However, government funding alone can only move the needle on semiconductor innovation so far. Increased collaboration between companies and research institutes across Europe is also essential.

In the case of EV Group, since our founding more than 40 years ago, we have been actively engaged with research institutes, universities, and suppliers across the semiconductor value chain in Europe. These collaborations give us access to world-class expertise to develop key technologies and apply our leading-edge solutions to address real-world industrial applications. A central tenet to our Triple-i philosophy of "invent-innovate-implement" is our focus on engaging with world-leading organizations to accelerate the development and commercialization of new technologies that drive future innovations in the semiconductor industry. Here are a few examples of important collaborations we have undertaken with leading European organizations, many of which are backed by EU-funded projects:

Imec – EVG and imec have been strategic technology partners for years with a key focus on developing wafer-to-wafer fusion and hybrid bonding. Our collaborations focus on a system-level holistic approach, where all influencing factors are considered to scale integration and effectively reduce interconnect pitches. Among the influencing factors, the design of hybrid bond contacts is investigated along with dielectric materials as well as the copper properties of the pads. Even variations of wafer shapes are modulated to simulate the impact of different device wafer setups in logic, DRAM, and 3D NAND flash. Recently at the 2024 IEEE Electronic Components and Technology Conference (ECTC), EVG and imec reported achieving wafer-to-wafer direct hybrid bonding with electrically yielding interconnect pitches down to 400nm[7]

In addition to 3D SoCs, EVG and imec are also collaborating on the scaling of fusion bonds for 3D stacked devices. Besides being used for backside power delivery networks (BSPDN) for splitting signal lines and power lines of a transistor into different planes using wafer-to-wafer bonding, fusion bonding is being explored further for more futuristic devices. One example is complementary FETs (CFETs), which could be the first stacked transistors to use wafer-to-wafer bonding to enable efficient integration of nMOS and pMOS on top of each other. Another successful development is the transfer of transition metal dichalcogenides (TMDs), a class of atomically thin, layered semiconductor materials, which are even further out and discussed to be implemented by 2035 as a replacement for the pMOS in CFETs to enable even greater performance increases. In a joint paper at the 2024 Symposium on VLSI Technology and Circuits, EVG and imec demonstrated the successful transfer of high-quality tungsten disulfide (WS2) as a TMD material on 300-mm wafers[8].

Recently, our joint development activity has focused on EVG's LayerRelease technology, a novel IR laser release method. In this collaboration, the co-optimization of films and integration processes is conducted simultaneously. This enables the LayerRelease process to replace mechanical debonding with IR laser release in packaging processes. More importantly, LayerRelease enables full integration capability in front-end-of-line processes as it is 100 percent front-end process compatible. Imec's extensive integration and application-based research significantly benefit the technology, making it a unique setup in Europe and a leader on a global scale.

Fraunhofer – Fraunhofer has been another close research partner for many years, and EVG has collaborated with Fraunhofer in several areas, including UV laser debonding for heterogeneous wafer-to-wafer and die-to-wafer integration, as well as wafer-to-wafer hybrid bonding for system integration. Fraunhofer is also among our partners that utilize our centers of excellence such as the Heterogeneous Integration Competence Center (HICC) to complement customer development in their cleanrooms. Working together at our HICC, several industry-first device implementation flows have been generated and successfully transferred to European customers.

CEA-Leti – CEA-Leti's fundamental research in the field of wafer bonding and other process-relevant influencing factors complements EVG's own development work. A clear example of this collaboration is based on a high-vacuum bonding technology called EVG ComBond. Various new types of oxide-free material compounds are being researched in this field in order to enable conductive, transparent and atomically smooth bond

connections. While CEA-Leti is primarily researching the material transitions and fundamental mechanisms of bonding, EVG's focus is on optimizing the application and further developing the hardware[9,10]. (Figure 3)

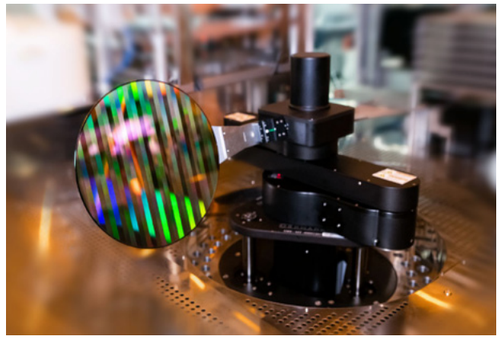


Figure 3: Robot handling a 300-mm wafer in an EVG system installed at LETI's cleanroom. ©Andréa Aubert/CEA.

Another example among many is the relationship between dielectrics and bond strength. Especially in the area of low bonding temperatures, dielectrics and activation in the bonder play an increasingly important role. A precise understanding of bond strength, adhesion, and adherence, as well as the associated effects and potential defects, is essential to guarantee the highest process yield and bond stability[11]. Particularly within these fundamental research topics, CEA-Leti generates high value.

Another important field of research was realized as part of a collaboration between CEA-Leti, ASML, and EVG. The fundamental relationships between bonder-induced overlay data, process-induced distortions, and distortion compensation in the scanner were investigated. Using high-resolution data, bond distortions could be efficiently optimized to meet the compensation possibilities of lithography. In this co-optimization, an overlay of less than 10nm was demonstrated, which is essential for BSPDN and subsequent sequential 3D integration.[12,13]

Conclusion

Europe is ushering in a new chip renaissance thanks to renewed public focus and investments in its domestic semiconductor industry coupled with Europe's historical strengths in leading-edge research and key process areas that are fueling semiconductor innovation. Besides funding, increased collaboration between companies and research institutes across Europe is essential to making this renaissance a reality, and we are witnessing many examples of this today. It is truly an exciting time to witness this revival in the making.

References

1. European Commission, Press Release, "Commission launches Chips Joint Undertaking under the European Chips Act," November 30, 2023, https://ec.europa.eu/commission/presscorner/detail/en/ip_23_6167
2. NanoIC, Website, "NanoIC pilot line technologies," https://www.nanoic-project.eu/en/technologies
3. FAMES, Website, "TECHNOLOGIES," https://fames-pilot-line.eu/technologies/
4. The Finnish Chips Competence Center (FICC), Website, "Pilot Lines," 2024, https://www.ficcc.eu/pilot-lines
5. Filippo Di Giovanni, Power Electronics World, "Europe approves a project for an advanced chip pilot line in Catania, Italy," April 15, 2024, https://www.powerelectronicsnews.com/europe-approves-a-project-for-an-advanced-chip-pilot-line-in-catania-italy/
6. European Commission, Press Release, "EU invests €65 million in quantum chips," September 24, 2024, https://digital-strategy.ec.europa.eu/en/news/eu-invests-eu65-million-quantum-chips
7. B. Zhang, et.al., "Scaling Cu/SiCN Wafer-to-Wafer Hybrid Bonding down to 400 nm interconnect pitch", 10.1109/ECTC51529.2024.00058
8. S. Ghosh, et.al., "EOT Scaling Via 300mm MX2 Dry Transfer - Steps Toward a Manufacturable Process Development and Device Integration", 10.1109/VLSITechnologyandCir46783.2024.10631364
9. K. Abadie, et.al, "Vacuum Quality Impact on Covalent Bonding", 10.1149/MA2023-02331600mtgabs
10. Q. Lomonaco, et.al., "Stress Engineering in Germanium-Silicon Heterostructure Using Surface Activated Hot Bonding", 10.1149/MA2022-02321219mtgabs
11. K. Abadie, et.al. "Study and Control of the Distortion Induced by the Bonding Process for BSPDN Approaches", 10.1109/IITC61274.2024.10732379
12. Richard van Haren, et.al., "Enabling layer transfer and back-side power delivery network applications by wafer bonding and scanner correction optimizations", 10.1117/12.2657422
13. Richard van Haren, et.al., "Characterization and mitigation of local wafer deformations introduced by direct wafer-to-wafer bonding", 10.1117/12.3010477

The "White House of Microelectronics Packaging" Celebrates Its 15th Anniversary!

By Juliana Panchenko and Frank Windrich, Fraunhofer IZM-ASSID

15 years ago, Fraunhofer established a leading-edge research center for 3D integration and advanced wafer-level packaging on 200/300mm wafer sizes. It was founded based on visionary ideas in the field of microelectronic packaging from the former director of Fraunhofer IZM, Prof. Herbert Reichl. Supported by the Free State of Saxony, the Federal Ministry of Education and Research (BMBF) Germany, the European Commission, and the Fraunhofer Society the Center "All Silicon System Integration Dresden - ASSID" was founded directly in the heart of Silicon Saxony in a fully industry compatible clean room environment (Figure 1).

Figure 1: Fraunhofer IZM-ASSID "The White House of Microelectronics Packaging"

It was the first 300mm R&D facility for this purpose in Germany. The first three years were dedicated to upgrading the "White House" clean room from a back-end chip-scale packaging facility to a leading-edge 3D integration facility, at a time when the mainstream industry was focusing on chip-scale packaging and embedded wafer-level ball-grid array (eWLB) technology.

The focus in the early years of the small, strong, and motivated researcher team was to develop advanced wafer-level packaging technology building blocks in 2.5D / 3D integration. In cooperation with local 300mm foundry partners, through silicon vias (TSV), re-distribution layer (RDL) and micropillar interconnect technologies were developed and transferred to volume production. All required technology building blocks for 2.5D / 3D integration starting from wafer bonding and thinning, multi-layer RDL in Cu damascene and polymer flavor, TSV formation, interconnect fabrication, die assembly, and in-line metrology were set up to form a leading-edge industry-compatible 200/300 mm heterogenous 3D wafer-level system integration pilot line.

The past 15 years have brought numerous scientific projects and industrial cooperations with institutions all over the world. The first years were focused strongly on the above-mentioned topics on the development of Cu TSV processes and 2.5D silicon interposer fabrication with flip-chip micropillar interconnects. A key R&D project was CarrICool leveraging the integration of an active cooled Si interposer with TSVs surrounded by fluidic channels for advanced thermal management in high-performance computing applications (Figure 2).

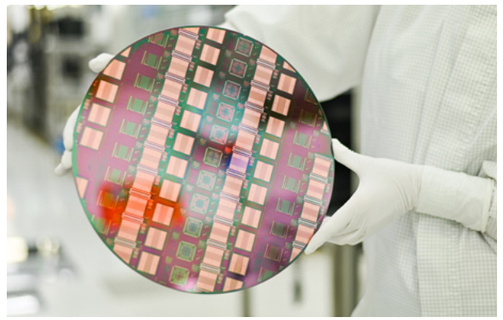


Figure. 2: Si interposer wafer with fluidic channels for active cooling (© Photography by Silvia Wolf)

The expertise in Cu TSV technology opened up the integration of TSVs in custom ASIC devices by TSV's last 3D integration. Such an integration approach allows leading-edge systems in package (SiPs) for various detector and sensor applications in the medical and industrial fields.

To support the industrial demand for small- and mid-size volume pilot line manufacturing, an ISO 9001 quality system was established in 2014. The middle and end of the decade were focused on extending the wafer-level packaging capabilities to address different markets.

We focused on technology development for RDL1st fan-out wafer-level packaging with multi-die embedding to build highly miniaturized SiPs. The technology was used to develop a universal sensor platform. Furthermore, the integration of Cu/Cu hybrid bonding technology was investigated at a very early stage in the development. Activities to develop the packaging of a full 300 mm wafer-scale integrated high-performance computing system were also realized.

The time is running extremely fast and in semiconductor R&D even faster. Today we see real 3D integration in numerous products driven by the artificial intelligence (AI) and high-performance computing (HPC) market. We see Si interposers in high-volume manufacturing and are in the era of chiplet integration. The industry has wafer-scale computing systems for big data AI applications in the market and we believe that Interconnectology will be the future.

Continued on page 70

Witnessing Foundry 2.0 in Action

By Françoise von Trapp

One way I learned about advanced packaging technology and what it entails is by visiting our community member companies. There's nothing like talking to the experts face-to-face and walking through a cleanroom or advanced packaging applications lab to drive home a concept.

For the past year, I've been talking with Bob Patti, Founder and CEO of NHanced Semiconductors, about the company's growth and expansion in North Carolina and Indiana and the launch of a new business model he calls Foundry 2.0. Recently, Patti invited me to the Morrisville, North Carolina facility to get a first-hand look at Foundry 2.0 in action.

Who is NHanced Semiconductors?

Coming up on its 9th anniversary, NHanced Semiconductors spun out of Tezzaron Semiconductor in 2016 to focus on the high-end advanced packaging technologies that Patti and his team of design and packaging engineers first developed at Tezzaron. The team pioneered layer transfer stacking for DRAM memory.

Patti is a serial entrepreneur—having founded nine start-ups, including Tezzaron and NHanced. While he hails from chip design, he says his experience over the years has shaped him into an advanced packaging process engineer. He likes to say that NHanced specializes in leading-edge technology from 25 years ago.

So what does he mean by that? It's simple: the company implements 25-year-old fab technology that is leading-edge for advanced packaging today. Advanced packaging isn't done at the nanometer scale, he explains, so using advanced node processes and processing equipment for 2.5D interposer fabrication and 3D IC stacking is overkill (Figure 1).

Figure 1: This Class 1000 cleanroom is outfitted with 200mm CMP tools.

"Moore's law is dead, in terms of cost," Patti says. "We can continue scaling but it's expensive. Advanced packaging allows us to eliminate unused elements and reduce the transistor count, which directly reduces cost and power, and still meets or exceeds the needed performance."

He's talking about the processes and technologies that will enable next-generation chiplet architectures, as well as complex systems-in-package (SiP) for specialty applications.

"All advanced packaging really boils down to is getting rid of the wire," says Patti.

What Is Foundry 2.0 and Why Do We Need It?

Foundry 2.0 sources dies and chiplets from traditional foundries and applies semiconductor foundry processes and advanced packaging and assembly technologies. It uses front-end processes such as photolithography, chemical mechanical polishing (CMP), deep reactive ion etching (DRIE), and hybrid bonding processes. The results are highly interconnected 2.5D interposer assemblies, 3D stacked ICs, and chiplet configurations.

What makes Foundry 2.0 different from Foundry 1.0?

Patti explained that while traditional foundries and IDMs implement 2.5D and 3D advanced packaging for chiplet integration internally, they can't serve customers who want to tap into these technologies to integrate third-party chips—memory, for example—into the package. They also aren't interested in customization or low-volume applications.

"Foundry 1.0 operates on the theory: You can get any color you want, as long as it's black," says Patti, as an analogy. At NHanced, you actually can get any color you want. And because NHanced doesn't make transistors, it's not competing with its customers. The company partners with all the leading-edge foundries to source its chips, then adds its magic to turn them into custom devices.

Another key differentiator between Foundry 2.0 and Foundry 1.0 is reduced manufacturing cost. By using legacy tools and processes for the basics and reserving the leading edge for the "special sauce," Patti says he can keep the cost down lower than what the tier-one foundries and IDMs can do.

The timing couldn't be better for NHanced and Foundry 2.0. The semiconductor industry is changing, driven by the needs of artificial intelligence (AI) and other high-performance computing applications. Rather than being volume-driven, it's now value-driven.

"The profit margins for fabs and IDMs are taking a hit, and the end users like NVIDIA are seeing the profits. If we continue to rely exclusively on Foundry 1.0, the costs of semiconductor devices will continue to increase, and so will the cost of our end devices," notes Patti.

The Birthplace of Hybrid Bonding

The facility in Morrisville, North Carolina, where I visited, is also the birthplace of hybrid bonding. It was invented in this building by Ziptronix (now Adeia) by Gill Fountain and Paul Enquist. Fountain still shares office space with the NHanced team. NHanced bought the building in 2017, along with a full technology transfer license from Adeia, and is now the first company to implement hybrid bonding in its processes for heterogeneous materials like silicon and glass, and silicon carbide.

The cleanroom space is outfitted with mostly refurbished equipment; workhorses that excel in performing legacy node processes that are well suited to the feature sizes for the most advanced packaging processes (Figures 2, 3).

Figure 2: This Class 1000 etch bay is outfitted with customized equipment, such as this dual chamber, silene based oxide deposition system.

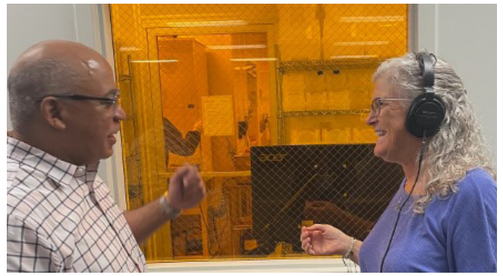


Figure 3: Carl Pettaway gave me a "window" tour of the North Carolina clean room. Here, were looking into the lithography bay of the class 100 cleanroom.

But when a process calls for a new, leading-edge tool, Patti happily invests in it. For example, the company recently bought one of the first Besi Datacon 8800 CHAMEO systems for room-temperature direct fusion and hybrid bonding processes. (Figure 4).

Figure 4: The Besi Datacon 8800 CHAMEO ultra plus is an advanced room-temperature hybrid bonding system that addresses increased demands for performance, speed, accuracy, and warpage control in fine-pitch copper interconnects with submicron pad sizes.

Patti says the company does virtually all the advanced packaging for the federal government that requires hybrid bonding.

"The good news is we're drowning in business," says Patti. "For hybrid bonding, our facility will be able to produce larger volumes than TSMC by 2026."

Expansion Plans for NHanced

NHanced is 100% self-funded. There are no investors and no debt. And while NHanced was in the running for CHIPS Act funding, Patti believes they were passed over primarily because the model he proposed targeted lower-volume production rather than typical OSAT high-volume manufacturing.

But this hasn't stopped Patti's plans for expansion. Up until now, NHanced has been primarily a development company but is now ramping up to become a volume manufacturer of high-mix devices. Patti anticipates that the company, which has seen 10x growth in the last two years, will see another 10x increase in revenue over the next five years.

Growth plans are in motion. Patti's excited to partner with governments in Indiana and North Carolina to implement those plans, along with local researchers like the Applied Research Institute and academia including North Carolina State University, Ivy Tech, and Purdue University.

Headquartered in Illinois, in 2023 NHanced invested in a volume production advanced packaging facility in Odon, Indiana. The ribbon cutting was in January, and the building and cleanrooms are complete and will soon house a new interposer fabrication line capable of 5,000 wafers per month, operational by early Q1 2025. This complements its existing line, which is ramping up to two and then three shifts.

While he was originally eyeballing a second Indiana manufacturing site to further implement Foundry 2.0, he has now pivoted to focus on expanding the existing North Carolina location.

"By 2026, we'll add two more 5,000-wafer lines in North Carolina—one for 300mm and another for 200mm wafers. Altogether, we're targeting 15,000 to 16,000 wafers per month by the end of 2026." says Patti.

The site currently produces 250 wafers per month (wpm) —but orders are exceeding capacity. So they are adding a second shift, expanding the cleanroom footprint, and installing automated 200mm and 300mm tool lines to accommodate volume production. This includes the aforementioned BESI CHAMEO. (Figure 4)

“The increased throughput of the new Besi system translates to lower cost for our customers,” said Patti. “Even more exciting is the improved yield, which will allow us to handle much larger assemblies economically. I expect to see new products containing dozens of chiplets.”

Expansion plans in Indiana and North Carolina are expected to bring high-paying jobs to the regions. Realizing that technician jobs in an advanced packaging foundry are specialized, Patti says they offer extensive training and above-average pay. “These investments provide long-term return because employees tend to stick around,” he says.

What the Future Holds for Foundry 2.0

Patti predicts a paradigm shift for the semiconductor industry. He envisions a future where microelectronic devices are more customized and transistors are fewer but more powerful. He hopes that Foundry 2.0 is a concept that other companies adopt. Patti hasn't patented the phrase. He's just setting the example for other players in the industry. It's time for all companies like NHanced, which excel in customization, to thrive.

To hear Patti describe Foundry 2.0 in his own words, listen to the podcast. We also take an audio tour of NHanced's North Carolina cleanrooms, guided by operations director Carl Petteway.

Why North Carolina?

“North Carolina’s targeted, performance-based incentive programs help companies and communities grow and thrive in our state.” says Katy Parker, Director of Project Management at the Economic Development Partnership of North Carolina. “In situations where North Carolina is competing with other attractive business locations, our competitive incentive programs can come into play.”

The Job Development Investment Grant (JDIG) is a performance-based, discretionary incentive program that provides cash grants directly to new and expanding companies to help offset the cost of locating or expanding a facility in the state.

The One North Carolina Fund (OneNC) is a discretionary cash-grant program that allows the governor to respond quickly to competitive job-creation projects. The North Carolina Department of Commerce administers OneNC on behalf of the Governor. Awards are based on the number of jobs created, level of investment, location of the project, economic impact of the project and the importance of the project to the state and region.

More than 330 electronics manufacturers call North Carolina home, and the state’s universities graduate 500 electrical/electronics engineers and 420 computer engineers annually. Additionally. community colleges offer customized training for new and expanding manufactures. Because of these factors, 38 companies in electronics manufacturing have located to or expanded in NC since 2021, totaling over $17 billion (Toyota is $13 billion of this) in capital investment and over 10,300 new jobs, says Parker.

As a place to live and work, North Carolina has one of the fastest growing populations in the country. Racial diversity is also on the rise. Parker says the housing market is strong with increasing supply. The average home costs around $330,000. The region also reportedly boasts a strong education system.

Picking up the Pace of Panel-level Advanced Packaging at Onto Innovation

How a Collaborative Partnership is Accelerating PLP Innovation

By Françoise von Trapp

Monita Pau, Danielle Baptiste, Keith Best, Mike Plisinski, and Jason Robinson cut the ribbon to officially open PACE.

Panel-level advanced packaging technologies have been in development for more than a decade. They began as a way to reduce costs and improve yields for fan-out wafer-level applications. Smartphone applications—particularly fingerprint sensors—promised volumes that would make the investment successful.

However, memories of the fiasco of 450mm wafer efforts lived in the minds of many. Why invest in an ecosystem that may not demand high enough volumes to ensure a return on investment? Still, there were those who believed in the promise of panel-level packaging. Development efforts have persevered, and PLP has moved through R&D and into pilot production. Still, through it all, many remained skeptical about there being high enough volumes to support it.

The Era of AI, coupled with the emergence of glass substrates, is set to change all that.

On September 30, 2024, I visited Onto Innovation's headquarters in Wilmington, MA to attend the grand opening of its Packaging Applications Center of Excellence (PACE). The company has partnered with like-minded suppliers of the PLP ecosystem to accelerate the development of PLP technologies for both organic and glass substrates. These include 3D InCites members: LPKF Laser & Electronics, Evatec, MKS-Atotech, and Lam Research; as well as Resonac, Corning, and others.

Figure 1: District Director Janice Phillips presented a senate citation from the office of Massachusetts Senator Barry Finegold to Mike Plisinski, chief executive officer of Onto Innovation. In the citation, the senator congratulated Onto Innovation for the grand opening of the Packaging Applications Center of Excellence and gave his support for future success.

I spoke with CEO Mike Plisinski (Figure 1) and toured the PACE facility with its director Keith Best. I also connected with attendees from LPKF, Corning, Evatec, MKS Atotech, and Resonac to learn more about PACE's mission. Lastly, I spoke with Dave Robertson, Massachusetts State Representative for Wilmington and nearby Tewksbury about the support the State of Massachusetts gives to the microelectronics sector.

What's Driving Panel–level Advanced Packaging?

“The ERA of AI is the most transformative era in our lifetime,” said Plisinksi. “It has the potential to be as transformative as electricity or the Internet,” echoing what Jamie Dimon, the CEO of JPMorgan Chase, conveyed in his annual shareholder letter earlier this year. He added that it goes far beyond revenue growth for the semiconductor industry. It's the impact AI will have on society and the issues it can solve.

Over the past year, demand for AI chips has increased dramatically, driven by generative AI applications. One company, Nvidia, is emerging as the "king of the industry", and its efforts to increase processing power led them away from the latest generation of front-end transistor technology.

"Nvidia leveraged advanced packaging to provide the processing and compute power necessary to unlock those AI algorithms,” noted Plisinski. Specifically, Nvidia combined 2.5D and 3D memory stacking to reduce interconnect distances and improve the power efficiency, device performance, area, and cost (PPAC) of the device.

While initially, these implementations were in wafer format, as AI chipsets increased in size, moving to panel format made sense to increase yield and reduce waste. It's the basic square-peg/round-hole dilemma.

One of the current challenges that the industry hopes will be solved with glass core substrates, is that silicon is not available in panel format. Achieving the high densities equivalent to that of silicon wafers means reducing line/space dimensions of redistribution layers (RDL) on both fan-out and interposer packages. Glass core substrates will also allow for finer features.

Enter the Packaging Application Center of Excellence

Keith Best, Director of PACE, took me on a tour of the facility, which is equipped with Onto Innovation’s lithography and inspection tools, a process lab, and software that connects data from Onto and third-party tools to provide insightful and actionable analytics and dashboards (Figure 2). He provided a step-by-step description of the processes as panels move from the photoresist coater to the lithography stepper, to the developer, and then to the inspection system.

Figure 2: An audio tour of PACE with director Keith Best.

Best said Onto Innovation decided to focus efforts in PACE on PLP because package sizes are growing to 100mm and beyond. "Customers are talking about package sizes of 150mm, which means that wafers will no longer be relevant in this space, and packages need to be built on panels."

The collaboration partners are part of a virtual line. Lithography processes happen at PACE, and the panels are shipped to, for example, Evatec for seed metal deposition and Lam Research for electroplating, and then back to PACE for inspection.

“Everyone in the collaboration will benefit by having access to next-generation chemistry, as well as next-generation lithography. Because you can’t plate 2-micron line/space unless you have an advanced packaging lithography tool," said Best.

Collaboration partners came together through conversations at events such as IMAPS DPC, with “adjacent OEMS who had the same mindset we had,” said Best. There is no fee to be part of PACE at the moment. Rather each one of the partners will have a statement of work with Onto Innovation, specific to the processes and/or materials they provide. By providing the “bookend” capabilities—leading edge lithography for sub-2-micron line/space, and then post-process inspection, Onto is making it possible to optimize panel-level packaging processes.

"We now have the capability to print large, wide-field packages that haven’t been coming to market for several years at 1-micron capabilities. For companies that wanted to invest in and see how their plating or chemistries perform with these more advanced structures, they had no way to test,” said Plisinksi.

He explained that PACE allows Onto Innovation to leverage its equipment, to print and image these structures and see how the plating adhesion works on glass. Furthermore, he added, the process control capabilities of the Firefly system make it possible for customers to learn develop, and characterize their process equipment and use Onto’s software to connect all the pieces together.

Why Join PACE?

Ralph Zoberbier, CMO of Evatec, said that being part of PACE gives the company a step forward as a viable supply chain partner. It also gives Evatec engineers the opportunity to gain experience and know-how while working with engineers at other companies. “We also want to enhance our products and are working on new generation panel PVD type of technologies," he added.

“Many semiconductor industry innovations occur at the intersection of materials and process equipment,” noted Junro Yoon, of Corning Advanced Optics. “We are excited by this partnership to uncover new innovations."

“As we move into the next generation of advanced packaging, it’s clear that no one company is an expert on all the different areas,” said Kuldip Jopal, MKS-Atotech. For MKS-Atotech, that translates to support in developing next-generation dielectric materials, and also collaboration on developing test vehicles to address finer pitch. Collaboration with Onto Innovation in PACE does that by gaining access to lithography and inspection tools that help in pre- and post-creation of fine lines and spaces.”

Richard Noack, LPKF, noted that joining PACE allowed the company to participate in an entire ecosystem focused on glass packaging. LPKF provides the laser-induced glass etch process to form through glass vias.

What's Next for PACE?

While immediate efforts will focus on bringing PLP on organic and glass substrates to high volume to support the growth in AI, the partners don't plan to stop there.

As customers clamor for even finer lines/spaces down to 1 micron, Best says they will need to consider other potential partners to support CMP, which currently is only in development for PLP.

Companies who are interested in joining PACE should reach out to pace@ontoinnovation.com.

To hear all the interviews from the PACE grand opening, be sure to listen to the podcast episode.

Continuing the "Mass Miracle"

Dave Robertson, Massachusetts State Representative for Wilmington and nearby Tewksbury, MA, also attended the grand opening. We talked about the advantages of building technology businesses in Massachusetts. He reminisced about the 90’s initiative dubbed “The Mass Miracle" when the northeast corridor became a technology hub, with companies like Cisco, Digital Equipment Corp, Wang Computers, Sun Microsystems, and others fueling demand for computer chips; and companies like Analog Devices designing them.

Recalling Massachusetts's strength in the industrial era, followed by a slump of offshoring, Robertson said the state's continued investment in technology makes it a great place for high-tech companies to set up shop. He also highlighted the education opportunities from K-12, noting that the state ranks among the top in the nation for education. He also talked about free community college for people over 25 seeking new workforce opportunities. On the downside, the region is plagued by a high cost of living, due to expensive housing and utilities. He said he hopes that with more companies like Onto Innovation coming in, that will help with costs.

Announcing the 2025 3D InCites Awards Finalists

By Avery Gerber

For the 2025 3D InCites Awards, we settled on three distinct categories: Technology Enablement, Engineer of the Year, and Best Place to Work. These categories highlight the incredible contributions and efforts made by companies and individuals within the semiconductor and advanced packaging industries.

The Technology Enablement Awards will honor companies that have identified and solved critical challenges in the commercialization and manufacturing of HI, 3D HI, and chiplet architectures, driving the industry forward through cutting-edge solutions and advancements.

Engineer of the Year recognizes one individual whose technical expertise, innovation, and leadership have significantly impacted the development and implementation of technologies that shape the future of semiconductor packaging and integration.

Best Place to Work will celebrate companies that have fostered outstanding work environments, where innovation, collaboration, employee well-being, and professional growth are paramount, creating spaces where employees thrive both personally and professionally.

All the finalists for these awards demonstrate exceptional commitment to pushing the boundaries of technology, promoting diversity, fostering strong workplace cultures, and driving the future of the semiconductor industry.

2025 3DInCites AWARDS
For Excellence in Heterogeneous Integration Technologies

Platinum Sponsors:

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Technology Enablement Awards

ACM Research

With the growing demand for AI applications requiring large chiplet GPUs and high-density HBM, the industry is shifting from traditional 300mm wafer packaging to larger substrates like 510x515mm or 600x600mm to reduce costs and improve efficiency. ACM Research's Ultra ECP ap-p system is the first commercial high-volume copper deposition tool designed for panel-level packaging, offering advanced solutions for processes like pillar, bump, and RDL plating. Its horizontal chamber configuration ensures excellent uniformity, minimizes contamination, and supports up to 16 plating chambers. The system is operational in cleanrooms, with additional units set for deployment to customers.

Resonac

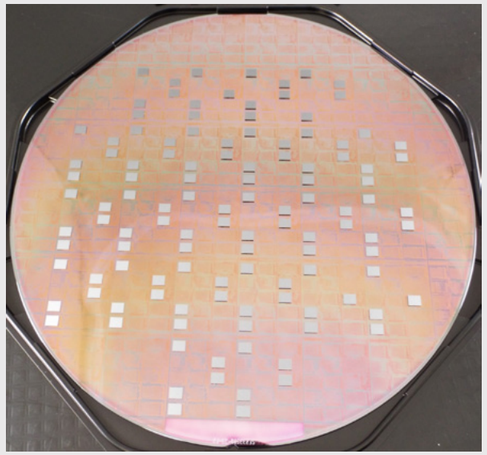
Resonac plays a pivotal role in advancing semiconductor performance through innovative packaging technologies and ecosystem collaboration. To address challenges in heterogeneous integration and chiplet packaging, the company developed the JOINT2 Consortium, which focused on fine pitch bonding, underfill materials, and advanced processes like semi-additive plating and polymer damascene. Achievements include successful 10 µm pitch bonding with flux-less technology and demonstrated 1/1 µm line/space capabilities.

Building on this success, Resonac is leading the US-JOINT consortium in Silicon Valley, partnering with 10 global manufacturers and institutions like the Texas Institute for Electronics to accelerate R&D in advanced packaging. This initiative fosters collaboration across materials, equipment, and design to fast-track commercialization and innovation.

Onto Innovation

Onto Innovation is driving advancements in chiplet integration and high-performance packaging with its Packaging Applications Center of Excellence (PACE) in Wilmington, Massachusetts. PACE focuses on co-developing next-gen architectures and packages alongside key industry partners, addressing challenges like shrinking line/space (l/s) requirements and the shift to glass core substrates for enhanced stability and electrical performance. The facility features Onto's JetStep® lithography system for sub-1.5µm l/s imaging, Firefly G3 inspection tools for glass panel metrology, and the Discover Command Center for AI-driven process controls. This collaborative ecosystem accelerate s innovation and supports the transition to high-volume manufacturing.

NHanced Semiconductor Inc.



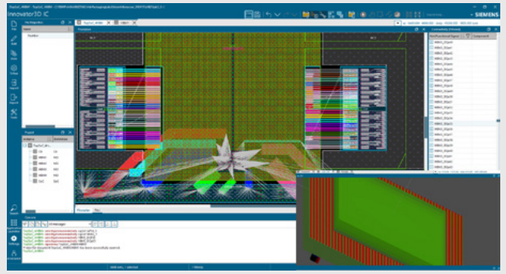
NHanced Semiconductor Inc. is revolutionizing heterogeneous 3D hybrid integration (3DHI) by overcoming challenges associated with integrating diverse materials like GaN, SiC, and LiNbO3. Using techniques such as incremental annealing and material thinning, NHanced achieves high-density interconnects with hybrid copper and covalent oxide bonding. These innovations enable the production of advanced 3DHI devices with unprecedented performance and power efficiency. By facilitating the integration of exotic materials, NHanced unlocks new possibilities, including intelligent AI-enabled IR sensors, advancing applications previously unattainable with traditional approaches.

Nordson Test & Inspection

Nordson Test & Inspection's revolutionary SpinSAM Acoustic Microscopic Imaging (AMI) system sets a new standard for wafer inspection in semiconductor manufacturing. With a compact footprint and unmatched throughput, SpinSAM scans up to four 300mm wafers simultaneously using proprietary non-immersion transducers, ensuring streak-free, high-resolution imaging while minimizing contamination risks. The system delivers complete wafer images without stitching in under six minutes, supporting diverse applications like bonded wafers and MEMS. Features like global tool matching, continuous operation, and efficient repairs streamline production, making SpinSAM a cutting-edge solution for high-yield, high-quality semiconductor inspection.

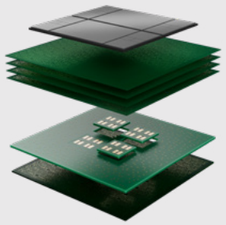
Siemens Digital Industries Software

Siemens Digital Industries Software is advancing 2.5D/3D IC heterogeneous integration with its Innovator3D IC platform, introduced in September 2024. This AI-enhanced co-design tool enables system-centric planning for die, interposer, package, and PCB design, ensuring seamless digital continuity. Innovator3D IC leverages predictive modeling for power, performance, area, cost, and reliability optimization, supporting interfaces like UCIe, HBM, and BoW. By providing early insights into thermal, mechanical, and electrical performance, it reduces design iterations and accelerates development. This comprehensive solution empowers engineers to create optimized, production-ready designs, transforming semiconductor design workflows.



Innovator3D IC is a 2.5/3D heterogeneous integration planning cockpit for multi-die and chiplet based semiconductor devices

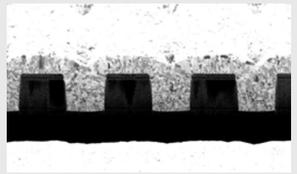
Saras Micro Devices



Saras Micro Devices is redefining power delivery for high-performance computing (HPC) and AI applications with its innovative STile embedded capacitor and voltage regulator solutions. These products enable embedded vertical power delivery (eVPD), reducing power delivery losses and improving efficiency by shortening the power pathway and minimizing the need for surface-mount components. This approach supports higher power densities in compact designs, unlocking the full potential of chiplet-based, multi-device architectures. Manufactured in Chandler, AZ, Saras collaborates with leading semiconductor suppliers to tailor STile solutions, accelerating design cycles and advancing integration for next-gen processors.

MacDermid Alpha Electronics Solutions

MacDermid Alpha Electronics Solutions addresses key challenges in heterogeneous integration (HI) and hybrid bonding with its NOVAFAB Fine Grain Copper electroplating process. Designed for high-density interconnects, this ultra-pure copper film ensures controlled grain growth during annealing, enabling defect-free bonds and enhanced device reliability. With a sub-2µm grain size, it minimizes signal degradation and meets the mechanical and electrical demands of advanced applications. Seamlessly integrating into high-volume manufacturing, NOVAFAB supports the performance and yield requirements of 3D stacking and chiplet integration, making it a reliable and scalable solution for next-gen electronics.



Engineer of The Year Finalists

Rex Anderson

Rex Anderson, PhD, Director of Operations at Micross, is leading the company's largest project under the DoD RESHAPE program: establishing a secure 300mm wafer bumping and finishing facility. With over 25 years of semiconductor expertise and a PhD in Nuclear Engineering from the University of Michigan, Rex has a track record of innovation at Applied Materials, Amkor, and RTI Microsystem Integration. His leadership on the SCAPEx project includes procuring and qualifying over 90 tools, overseeing complex facility modifications, and ensuring backward compatibility for diverse wafer sizes. Through meticulous planning and collaboration, Rex has kept the project on schedule and within budget, with the 300mm line set to launch by late 2025, solidifying Micross as a leader in advanced wafer processing.

Dmitry Padrubny

Dmitry Padrubny, Lead Application Engineer at Finetech, has over 20 years of experience in advanced semiconductor packaging, with nearly a decade at Finetech specializing in sub-micron die bonding for 2.5D and 3D integration. A graduate of Minsk Engineering College, Dmitry is instrumental in optimizing bonding processes for customers ranging from university labs to multinational corporations, addressing challenges in photonics, Lidar, Quantum, and AI. Recognized for his problem-solving and hands-on approach, he leads Finetech's North American technical team, mentoring colleagues and enhancing customer collaboration. Dmitry's contributions, including spearheading a cleanroom build for process development, drive Finetech's success in advancing heterogeneous integration from prototype to production.

Best Place to Work Finalists

Cadence

Cadence fosters a dynamic and inclusive workplace for over 12,000 employees across 25+ countries, driven by its "one Cadence, one team" culture. With a focus on continued learning and growth, Cadence hosts initiatives like the Cadence Women Conferences and offers competitive benefits, including bonuses, a stock purchase plan, and peer recognition, with 77% of employees honored in 2023. Beyond employee success, the Cadence Giving Foundation has committed $20 million to Fem.AI, promoting equity in the tech sector, and supports renewable energy with a virtual power purchase agreement for a U.S.-based solar farm. Cadence combines innovation, philanthropy, and sustainability to empower employees and communities alike.

EV Group

At EV Group (EVG), employees, or "EVG insiders," are at the forefront of turning innovative visions into real-world technology, shaping the future of industries like smartphones, medical technology, and virtual reality. The company thrives on its core values—Responsibility, Curiosity, and Trust—fostering collaboration across all roles, from administrators to field service engineers. Located in upper Austria's picturesque Innviertel region, EVG offers global company benefits such as flexible working hours, a company kindergarten, and health benefits. Emphasizing work-life balance, EVG organizes a variety of activities, and its EVG Academy provides comprehensive training for new employees. With a strong focus on curiosity and hands-on innovation, EVG continues to expand and seeks practical thinkers to join its growing global team.

Excillum

Excillum offers a dynamic and collaborative environment that fosters innovation, making it an exceptional place to work. As an R&D-intensive company focused on advancing X-ray metrology, Excillum empowers its employees to contribute meaningfully to developing cutting-edge X-ray sources. The company's culture emphasizes transparency, creativity, and teamwork, while also offering competitive compensation, comprehensive benefits, and a strong focus on work-life balance. Located near Stockholm, Sweden, Excillum combines the energy of a fast-growing tech hub with the tranquility of nature, creating an inspiring space for personal and professional growth. At Excillum, employees drive technological advancement while thriving in an inclusive and supportive workplace.

Koh Young

Koh Young is an exceptional employer, with innovation, teamwork, and personal growth at the core of its values. By leveraging cutting-edge technology and offering global opportunities, the company empowers its employees to shape the future together, creating a collaborative and forward-thinking environment that supports both professional development and meaningful contributions to the industry. The company offers tailored training programs to enhance everyone's skills and potential, and promotes a flexible, open, and inclusive workplace atmosphere, encouraging the exchange of ideas and respectful communication at all levels. A sustainable work culture and benefits that prioritize employees' well-being, health, and work/life balance make Koh Young a place where personal and professional goals align, creating an environment where employees can truly thrive.

Saras Micro Devices

Saras Micro Devices is a great place to work, known for its inclusive, dynamic, and thriving environment that fosters continuous learning, professional development, and employee well-being. Innovation through collaboration is central to the company's culture, where cross-functional teams work together, and diverse perspectives drive progress. Saras celebrates DEI&B and creates a sense of community through team-building activities and community outreach initiatives. The company supports work-life integration with flexible hours and generous paid time off while offering competitive salaries, benefits, and performance bonuses. Saras values its employees through peer recognition and rewarding milestones with unique experiences, making it a place where careers flourish and employees feel truly valued.

From Words to a World of Chips:
My Experience with IMAPS and The International Symposium

By Camden McCrea, Texas A&M

Recently, I worked on a grant proposal for the International Microelectronics and Packaging Society (IMAPS) Academy, as part of the Department of Commerce's National Semiconductor Technology Center's (NIST) workforce development initiative. Through this project, I experienced the semiconductor industry on a personal, first-hand level, working closely with IMAPS staff and committee members who are leading professionals in the industry (Figure 1).

Figure 1: Getting to know all the different people through DEI Bingo at the IMAPS Welcome Reception.

IMAPS is a global organization advancing microelectronics, packaging, and related technologies. Through a collaborative network of industry professionals, researchers, and educators, IMAPS fosters innovation and drives solutions that meet the demands of modern electronics. The society is a pivotal platform for knowledge exchange, training, and professional development, supporting the growth and evolution of the microelectronics field worldwide.

Through my work with IMAPS, I had a unique vantage point to witness and contribute to the semiconductor industry's critical alignment with government initiatives. This partnership is poised to shape technology on not only the national but global scale. The government's focused interest in the semiconductor industry and its extensive onshoring efforts underscored the sector's critical importance.

This exposure sparked a strong desire to deepen my understanding; if the government views this field as essential, it's worth my investment as well. As I am a newcomer to the industry, working on this proposal continuously sparked a keen interest, and showed me the personal and relatable side to semiconductors and the industry itself.

I witnessed IMAPS' strong commitment to the future of the workforce, as it makes significant efforts to engage and cultivate the next generation of industry professionals. Writing on their behalf exemplified this commitment, as they entrusted this project to me, someone new to the field yet eager to contribute meaningfully to their vision. Every page I wrote, I found my passion and interest growing in what, to my age group, is a generally misunderstood and underappreciated industry.

As I helped craft the proposal to communicate the critical importance of semiconductor workforce development, I was captivated by the industry's complexity and impact. There's often a misconception that extensive STEM expertise is a prerequisite for contributing to the semiconductor field, but my experience writing this proposal challenged that notion. I was met with patience and support from industry professionals who were eager to share their knowledge. This welcoming environment, combined with my growing curiosity, reinforced that there's a place in this field for diverse perspectives and skill sets.

Because of my work on this project, the society invited me to attend its International Symposium on Microelectronics in Boston in September (Figure 2). The Symposium not only showcased the cutting-edge of microelectronics but underscored the collaborative drive behind every breakthrough in the field.

Figure 2: We were invited to attend the Leadership Gala as a thank you for all our hard work.

It was amazing to see the international side of the industry, and meeting people from places all around the world such as the United Kingdom, Japan, Scotland, Germany, Taiwan, and many more. Not only did this symposium provide a front-row seat to the relentless pace of innovation in the semiconductor field, but it also opened the door to the truly fun and fantastic professionals of the industry.

Every person I met was extremely welcoming and a pleasure to talk with; a true embodiment of the microelectronics community. Learning about the intelligent innovations someone could create, and then meeting them on a personal level was a real treat.

While the wonderful people of the industry made the greatest impression on me, the many presentations I attended by inventors and researchers also captured my attention. It was evident that the semiconductor industry doesn't just follow trends; it sets the pace for future technological landscapes. I heard about groundbreaking innovations that fostered both a deeper understanding and appreciation for the industry.

This passion extended to the exhibit halls, where I got to speak one-on-one with representatives from leading companies of the industry. Their interest and excitement about their company's products and technologies was contagious. They were all open to newcomers like me, and excited to share their part of the industry.

Contributing to IMAPS' project and attending the symposium reinforced my understanding of how semiconductor advancements are essential to our technological and economic resilience, and that the industry is crucial to our nation's future. Both experiences taught me a much deeper, personal level of the industry and both the fun and excitement that can accompany the pursuit of innovation in the industry.

Bridging the Semiconductor Talent Gap– The Role of the European Chips Act and Beyond

By Isabella Drolz, Comet Yxlon

The European Chips Act (ECA) is pivotal to Europe's strategy for technological sovereignty, aiming to strengthen the continent's semiconductor supply chain and foster innovation. However, a key obstacle remains: the projected shortfall of 350,000 semiconductor professionals by 2030. Addressing this talent shortage is critical for the ECA's success and requires a combined effort of policy initiatives and industry actions.

The Talent Shortfall: A Pressing Concern

To achieve its goal of capturing 20% of the global semiconductor market, Europe needs a significant increase in skilled workers. Current estimates suggest that by 2030, demand for semiconductor professionals will reach 600,000, but only about 250,000 individuals are expected to be available, leaving a gap of 350,000 experts. This shortfall not only threatens Europe's competitive edge in the semiconductor market but also hampers its broader technological and economic ambitions.

Forecast: Estimated talent gap in Europe's semiconductor landscape in 2030

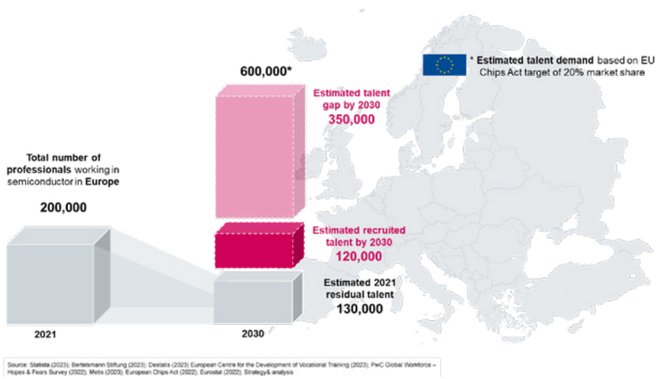


Figure 1: The EU semiconductro talent gap.

The European Chips Diversity Alliance (ECDA)

Next to other programs, a crucial player in addressing this issue is the European Chips Diversity Alliance (ECDA), headed by SEMI Europe. The ECDA aims to promote diversity, equity, and inclusion in the European semiconductor sector by strengthening ties between industry and education. By lowering barriers for underrepresented groups, the ECDA seeks to foster greater participation in the semiconductor workforce, addressing the missing talent critical to the growth and competitiveness of Europe's microelectronics industry.

By enabling collaboration between academia and industry, the ECDA is developing innovative training programs directly linked to EU standards. This methodology aims to assess the landscape of DEI in the European chips sector, pinpointing challenges and opportunities while shaping policy recommendations and actionable measures to drive change.

The ECDA is supported by a consortium of 11 partners from across Europe, representing industry, social partners, and higher education and vocational education and training providers. Key partners include companies like Merck, Comet, X-FAB, and educational institutions such as ECSP, EudaOrg and Comenius University Bratislava. The involvement of major industry players like Intel, Infineon, and GlobalFoundries further boosts the initiative's potential to bridge the skills gap while promoting long-term innovation through a diverse talent pool.

Building Brand Awareness

In addition to promoting diversity, semiconductor companies must focus on increasing brand awareness—an often overlooked but critical factor in attracting talent. The semiconductor industry, though foundational to modern technology, remains largely invisible to the public. This makes it difficult to attract skilled workers, especially those unfamiliar with the sector's vital role in everyday life, from powering smartphones to enabling renewable energy systems.

Raising public awareness about the importance of semiconductors is key to inspiring interest and drawing talent from diverse fields. Europe's automotive industry can be a role model here. The semiconductor industry could take inspiration from this sector, which has successfully built strong brand loyalty and inspired a passion for Europe's automotive brands and industry globally. With outstanding innovation, being part of something bigger, and thereby creating passion, could be also a winning strategy for the semiconductor sector.

Education and Industry Collaboration

Investing in education is essential for addressing the talent shortfall. The semiconductor industry should look again to the automotive sector as a model, where companies have partnered with universities to create specialized science, technology, engineering and math (STEM) programs that attract young talent. The semiconductor sector can replicate this by creating interest in its technology among students from a young age.

Educational initiatives should start early, engaging students from primary school through university. Why? Because making technology fun and accessible will create passion, which will set the foundation for future talents to enter the industry. In addition, programs that highlight the critical role semiconductors play in modern technology, such as workshops, summer camps, and competitions, can spark interest in the field. Additionally, offering scholarships and internships in partnership with semiconductor companies can provide students with valuable industry experience, further solidifying their interest.

Industry partnerships are crucial to achieving these goals. Under SEMI Europe's leadership in the ECDA, semiconductor companies collaborate with educational institutions and governments to create comprehensive training programs, mentorship, and career pathways. These initiatives will be inclusive, providing opportunities for individuals from diverse backgrounds to enter the semiconductor industry.

Moreover, the semiconductor industry needs to broaden its appeal beyond traditional engineering roles. The ECDA's focus on diversifying the workforce highlights the need for professionals in areas such as finance, marketing, service, operations, human resources, and many more. Promoting the industry as one that values a wide range of skill sets will help attract talent capable of meeting the sector's growing demands.

The Path Forward: Building a Sustainable Talent Pipeline

The projected semiconductor talent gap in Europe by 2030 is a significant challenge to the continent's technological ambitions. However, with targeted efforts from industry, education, and government, this gap can be closed.

In conclusion, the ECA and the ECDA are critical steps toward securing Europe's leadership in the semiconductor industry. However, to fully leverage these initiatives, the industry must place greater emphasis on brand awareness and its long-term benefits in attracting talent. By addressing the skills gap through education, increased industry and brand awareness, and a strong commitment to diversity, Europe can build a robust semiconductor workforce capable of driving innovation and ensuring technological sovereignty. The time to act is now, and the rewards—for Europe and the global community—are immense.

Face It: Live Events Strengthen Partnerships and Influence Product Innovation

By Ramachandran (Ram) Trichur, Henkel Semiconductor Packaging Materials

Conferences and industry trade shows have been the cornerstone of professional networking and educational advancement for as long as I can remember. More than 20 years ago, I attended my first semiconductor event, the Solid State Sensors & Actuators Conference (called Hilton Head 2002), and have been participating ever since. I still view these gatherings as a vital part of advancing product innovation, fostering commercial success, and contributing to my journey of discovery (Figure 1).

Figure 1: Henkel team networking in the Henkel hospitality suite at SEMICON Taiwan, 2024.

I'm grateful that our company also believes in their importance. Henkel's semiconductor electronics team participates in live symposiums—both in-person and online—around the world. They are unique opportunities to connect with the broader electronics community, share knowledge, collaborate with customers and industry colleagues, make new connections, and fortify relationships. All of this supports our product prioritization initiatives, business endeavors, and our team's professional development (Figure 2).

Figure 2: Henkel experts Rejoy Surendran, Yijia Ma and Ning Liu speaking on power electronics, advanced packaging, and FEA modeling, respectively, at various conferences in 2024.

The semiconductor manufacturing value chain is complex and globalized. Every end device made—memory, logic, analog, or others—has a specialized ecosystem for design, fabrication, and assembly. In most cases, the end device makers are different, with several key players in the West (North America and Europe) and a parallel ecosystem emerging in Asia for designing the components. However, manufacturing and assembly primarily take place throughout Asia. The decisions about design, development, and manufacturing are made across this global ecosystem. Because of this, participation at events around the world is critical to gain perspective on all actors in the supply chain, as there are regional differences in technological priorities, customer profiles, and required support.

The demonstrable and proven benefits are broad and significant, and Henkel's experience has substantiated the value of our participation. While there are numerous advantages, here are the top five things I believe live industry gatherings offer:

Identify Trends and Address Future Technology Needs

Data gathering for trend identification at trade shows and conferences informs potential development roadmaps. Visitor booth interactions pinpoint areas of interest and are documented. Data from all events globally is aggregated to assess the opportunity landscape.

These interactions help us to answer questions, such as: Are common trends aligning? Can we support them with a current solution, or is an innovation project needed? Additionally, important roadmap workshops are often co-located within these conference events. For example, at the Heterogeneous Integration Roadmap workshop, ecosystem players join forces to shape the future of advanced packaging. There are also valuable panel sessions centered around emerging technologies like glass substrates, co-packaged optics, and panel-level packaging that drive critical thought leadership considerations and industry actions.

Learn About Emerging Technologies and Our Potential Role

While the core competency in Henkel's semiconductor business is packaging materials development, often there are adjacent technical needs that perhaps our solutions can fulfill, or we have the technical know-how to develop. Conferences are a prime incubation ground for these conversations. We consider investable feasibility, strategic alignment, and growth potential and have a successful track record in this area. Connections with technologists at events have provided excellent insight for our recent work in supporting next-generation 2.5D and 3D package designs and bringing new advanced packaging underfill solutions to market. Other initiatives have also resulted in impactful materials development.

Explore and Solidify Partnerships and Alliances

Networking and relationship development are vital aspects of in-person events. Many of our collaborative semiconductor projects with academia, customers, associations, and other suppliers have been born at industry events. For instance, an RF packaging conference led to Henkel's and CITC's partnership to accelerate high thermal die attach progress. Often, these live interactions lead to the development of and/or participation in larger, multi-party consortiums and industry technology initiatives (Figure 3).

Figure 3: Henkel team members, Kefan Ni, Ram Trichur, and Rick Shen engaging with the media at Semicon China, 2024.

Collaborate with Diverse Ecosystem Participants

Henkel develops sophisticated semiconductor packaging materials, but they don't perform in isolation. Engaging with equipment suppliers, market analysts, ancillary material manufacturers, and process innovators provides tremendous value—sometimes with commercial success and always with essential learnings.

Showcase Technology Innovation and Team Talent

The exhibit setting allows a unique venue to present products in a differentiating way and facilitates an in-person deeper dive into conversation with customers and prospects. The display is the physical representation of our commercial portfolio where our technologists can discuss potential application solutions. Presenting papers at the conference gives us a forum to share our most innovative work and lets our product development and engineering experts receive valuable feedback and some well-deserved limelight for their contributions (Figure 4).

Figure 4: Henkel winning Supplier of the Year Award, presented by 3D InCites, at ECTC 2023

Recent papers at IMAPS 2024 in Boston, MA, on liquid molded underfill (LMUF) and Henkel's modeling capabilities for advanced packaging and technology presentations at this year's SEMICON China and SEMICON Taiwan have led to substantive discussions for development initiatives.

Conclusion

For Henkel, each event has a specific identity that determines its role in our participation level. Certain symposiums are more innovation-centered and technically rich and, therefore, provide excellent validation or insight for our product development initiatives. Other events satisfy explicit commercial goals to promote new products and connect with customers about project opportunities. Conferences and live symposiums have proven their value for many aspects of our business; our broad product portfolio, award-winning innovation record, top-tier expert staff development, and growing industry influence have all been enhanced by in-person engagement. Relationships matter, and Henkel is committed to building and fortifying them to enable the most impactful semiconductor technology solutions alongside our partners and customers.

Hope to see you at the next conference!

2024 IN PICTURES

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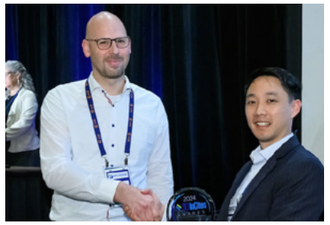



3D InCites Awards





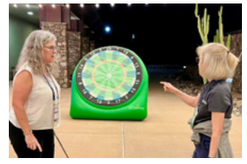







IMAPS Device Packaging Conference



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ECTC 2024

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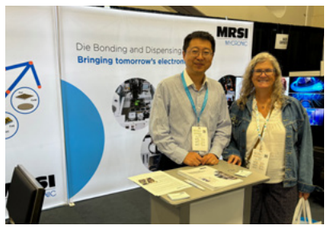

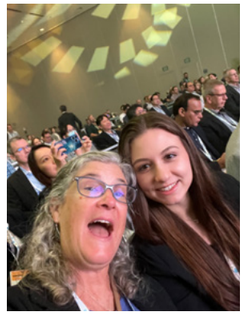

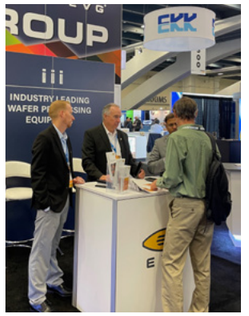



IMAPS Symposium 2024













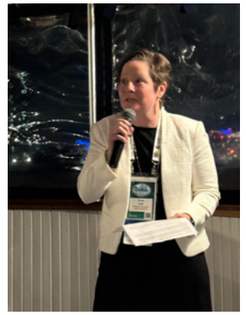
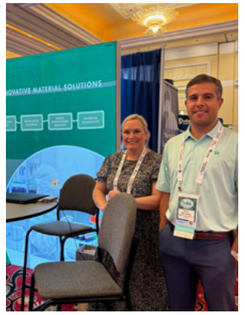


3D InCites Member Stammtisch 2024

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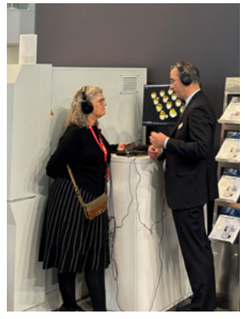

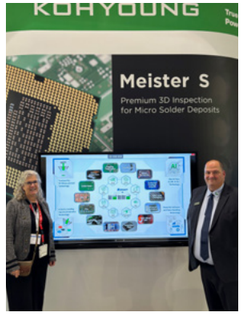

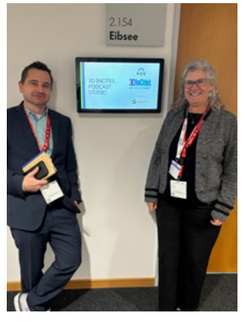

Cost-effective, High-performance Chips Are Driving the Move to Panel-level Processing

Continued from page 9

By utilizing fan-out techniques, designs can be made thinner and smaller, which is essential for modern consumer electronics. PLP integration can improve chiplet performance for the massive amounts of data being processed by AI, as well as in other compute-heavy applications. PLP also assists with the implementation of high-bandwidth memory (HBM) to help reduce compute times and power usage. Implementing PLP will also allow for more efficient package device design, as opposed to the more typical board-level packaging approach, which is the direction the industry is heading.

Enabling the Transition

New process equipment and panel handling is needed to make the transition to PLP. For example:

1. Electroless and electrolytic plating will be critical in building up the redistribution (RDL), pillar, and bumping layers to create the interconnects needed.
2. Panel bevel etching and cleaning in copper-related processes for both the front and back of the panel will help improve yield and remove metal contamination and residues that could cause electrical shorts.
3. A panel cleaning tool is needed that can remove flux and contamination from the center of the panel to eliminate void formation and prevent shorts.
4. And finally, a flexible panel handling system is required that can manage thin wafers and panels.

ACMR has developed process tools and substrate-handling systems to address these critical PLP process components to drive the future of packaging forward.

Summary

The transition from WLP to FOPLP reflects the industry's need for cost-effective, high-performance solutions that can meet the demands of modern electronics. As technologies evolve and the demand for smaller, more powerful devices increases, ACMR has been working with the industry to develop technology that will help FOPLP play a significant role in the future of semiconductor packaging.

US-JOINT Consortium: Strengthening Advanced Packaging Innovation Across Borders

Continued from page 27

Chet Lenox, part of KLA's industry and collaboration team, also shared KLA's perspective on the consortium's objectives. "Our main expectation is to work more closely with our partner companies—whether they are material suppliers or other equipment providers—to prove next-generation capabilities in an environment where we can share information freely without concerns over customer IP," said Lenox.

Lenox further elaborated on KLA's contributions to the consortium detailing what specific industry tools they specialize in and the company's goals to optimize efficiency through collaboration.

"We're contributing a direct imaging lithography tool for patterning wafers and panels," said Lenox. "One key goal is to co-optimize both the equipment and materials with suppliers, as successful lithography requires both elements to be finely tuned. This collaboration will accelerate our ability to optimize performance and deliver improved solutions to customers."

We also got the chance to speak with Kulicke & Soffa CTO Bob Chylak about how the collaboration will influence the pace and direction of technology development in semiconductor packaging.

"Traditionally, Japanese companies have a leading position for semiconductor packaging materials and substrates and U.S. companies excel at assembly equipment," said Chylak. The marriage of these will allow for the development of complete process flows with access to the latest R&D tools and materials. Combining these with engineering breakthroughs will increase the pace of packaging innovation in the U.S.

Beyond the technological advancements, the consortium strengthens ties between Japanese and U.S. companies, reinforcing collaboration in the highly strategic semiconductor sector. With the combined expertise of Kulicke & Soffa, NAMICS, KLA, and other members, the US-JOINT consortium is well-positioned to accelerate breakthroughs in semiconductor packaging and significantly impact the global supply chain.

The “White House of Microelectronics Packaging” Celebrates its 15th Anniversary!

Continued from page 33

It proves that the decision to start a leading-edge 3D integration research center 15 years ago was absolutely correct. Today's industry demand for advanced packaging solutions and 3D integration is bigger than ever. The number of microelectronic fabs located in Saxony around Dresden is increasing.

Today, Fraunhofer IZM-ASSID focuses on the fabrication of fine metallization structures to reach back-end-of-line (BEOL) structure sizes and develops new interconnect technologies for high-density assembly, wafer, and chip stacking based on various pitches using Cu/Cu hybrid bonding, microbumps for solid-liquid interdiffusion bonding as well as a new type of interconnect—copper nanowire bump.

Even if many 3D processes have been similar for 15 years, the devil is in the details. Small changes in the process sequence have an enormous influence on the full flow. The "White House" pilot line allows us to investigate these interactions between different technology steps.

Currently, the researchers are seeking new solutions based on chiplets for trusted electronics (Figure 3) and exploring packaging for quantum computing by incorporating new superconductive materials. Moreover, they built a bridge between applied research and academia via a strong scientific cooperation with TU Dresden and established a professorship for nanoelectronics materials in electronic packaging. Now students, Ph.D.s, researchers, and technicians work passionately in a family-like atmosphere of Fraunhofer IZM ASSID.

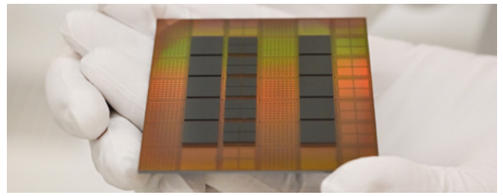

Figure 3: Assembled chiplet test vehicle with hybrid bonding for trusted electronics (©Photography by Silvia Wolf).

The upcoming years will bring rapid growth to the "White House of Microelectronics Packaging". The 3D wafer-level system integration pilot line will be expanded to a 2nd location to extend the 3D technology capabilities. The Center for Advanced CMOS & Heterointegration Saxony was founded with the Fraunhofer IPMS-CNT to bridge the gap for 3D between front-end and back-end wafer-level technology. Among other things, it will accommodate technologies in a 3D bonding hub to support multiple integration schemes for die-to-wafer and wafer-to-wafer system integration. The Center for Heterointegration has been a reality since June 2024!

Additionally, with four major European RTO partners (CEA-Leti, IMEC, VTT, and Fraunhofer), a multi-hub test and experimentation facility for edge AI hardware is in the realization phase. The PREVAIL consortium will allow cross-RTO processing in the field of 3D integration for edge AI applications. Once your design for a 3D system is ready, do not hesitate to come over and fabricate it on a 300mm wafer in the beautiful heart of Silicon Saxony at Fraunhofer IZM-ASSID!

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More information to come!

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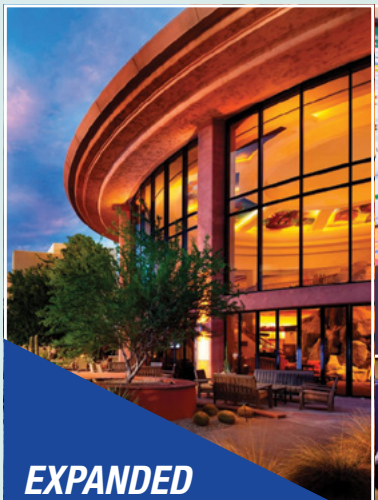

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